Extensible FPGA Framework (EFW)
For HiTech Global HTG-K7-PCIe Kintex-7 PCIE FPGA Module

Key Framework Features

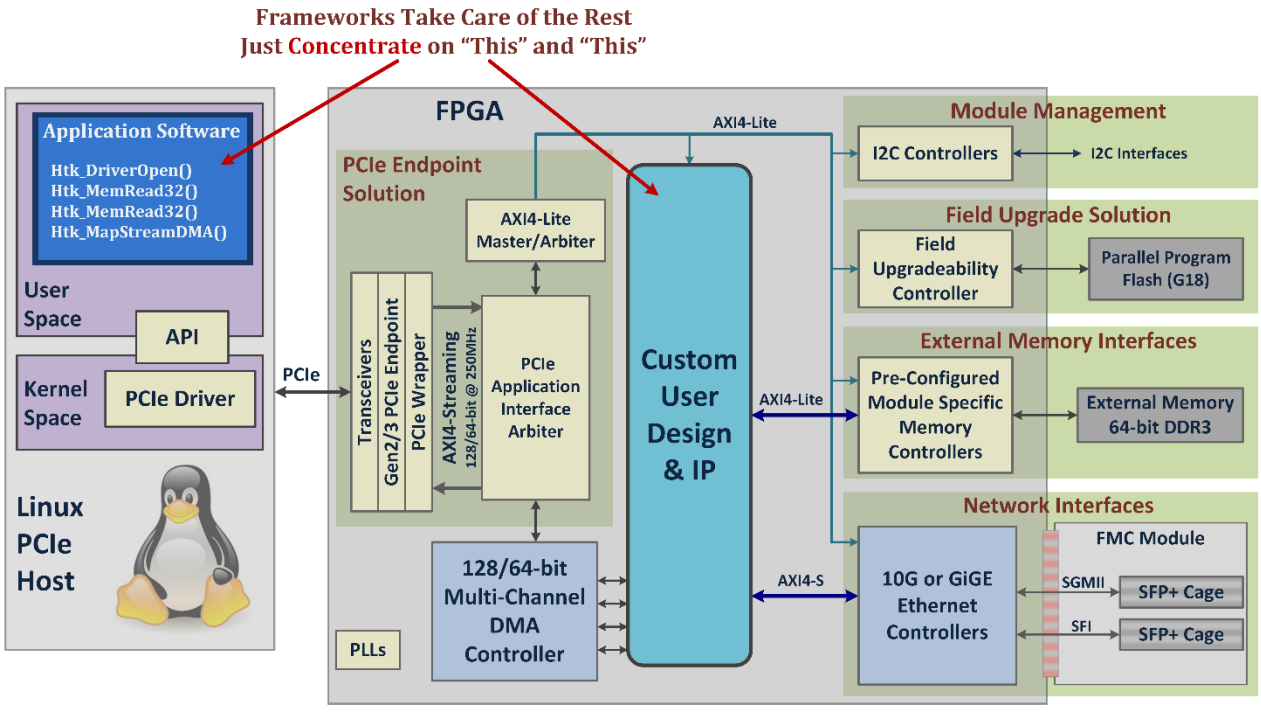
- Integrated, hardware verified solutions for 1G/10G Ethernet development
- HTG-K7-PCIe module targeted system building blocks of DMA Controllers, Ethernet MAC and PCS, PCIE application interface, AXI4 Interconnect, DDR3 and Flash Memory controllers
- Frameworks bundled with:
  - ***All options:*** x4/x8 PCIe Gen2 PCIe application interface, AXI4-Lite master/arbiter for memory mapped interface, Field Upgradeable (FUp) controller for in-system Flash programming and I2C controller
  - ***Selected Option Based:*** Synthesizable binaries and full simulation libraries for high performance (up to 32Gbps) multi-channel DMA controllers paired with GiGE, low latency 10G or ultra-low latency 10G
- Linux source code device drivers and APIs for PCIe interface and DMA controller
- Unified GUI for the entire EFW with scripting support
- Lowest startup cost for developing complete 1G and 10G solutions with Kintex-7 FPGA
- Simplified, single-sourced licensing for all FPGA IP cores and drivers

QUICKEST AND HIGHLY AFFORDABLE 1G AND 10G ETHERNET DEVELOPMENT WITH HTG-K7-PCIE MODULE

Extensible FPGA Framework (EFW) empowers FPGA developers with a verified set of productivity solutions, including module targeted physical interface components, device drivers and APIs for the HiTech Global HTG-K7-PCIE module.

Frameworks save months of development and debug time by enabling developers to skip the tedious and time consuming phase of IP core integration, interface verification and firmware development.

Framework Bundled Content	*Framework Type*			*Required FMC Module*
	Base	*1G*	*10G*	
Linux Device Drivers and APIs (Source)	●	●	●	-
x4/x8 PCIe Gen3 PCIe hard IP based PCIe application interface and arbiter (Verilog)	●	●	●	-
AXI4-Lite Master and Arbiter with 32-bit control plane for registers accesses (Verilog)	●	●	●	-
32-bit AXI4-Lite Slave for integrating user blocks (Verilog)	●	●	●	-
G18 Flash controller for in-system field upgrades (FuP) (Netlist)	●	●	●	-
I2C Controllers (Netlist)	●	●	●	-
Targeted DDR4 controllers with AXI4 wrapper (Verilog)	●	●	●	-
64-Bit 8-Channel PCIe RapidDMA with x4 Gen2 PCIe Endpoint (Netlist)		●	●	-
128-Bit 8-Channel PCIe RapidDMA with x8 Gen2 PCIe Endpoint (Netlist)				-
GiGE MAC with 1000Base-X Interface (Netlist)		●	●	FMC-X4SFP+
Low and Ultra-Low Latency 10G Ethernet, 32-bit data path (Netlist) ***Latency optimized for financial market applications***			●	FMC-X4SFP+ FMC-SFP-OC FMC-X2QSFP+



Productivity Features

PCIe Bus Interface and Management: Complete PCIe solutions for the HTG-K7-PCIE x4 Gen2 and x8 Gen2 PCIe interface. Framework implements up to two application side interfaces, a 32-bit AXI4-Lite compliant register access interface for Non-DMA (single read/write) operations and 128/64-bit AXI-4 streaming compliant interface for DMA operations.

Parameterized AXI4-Lite Inter-connect: Complete, fully parameterized 32-bit AXI4-Lite inter-connect with Master, Arbiter and Slave in source (Verilog) code for register access

High Performance PCIe DMA: 128-bit and 64-bit data path @ 250MHz (up to 32Gbps/16Gbps), multi-channel scatter-gather RapidDMA IP with AXI4 compliant user interface for high performance and low latency data transfers between host and module. Support for both Legacy and MSI interrupt mechanisms.

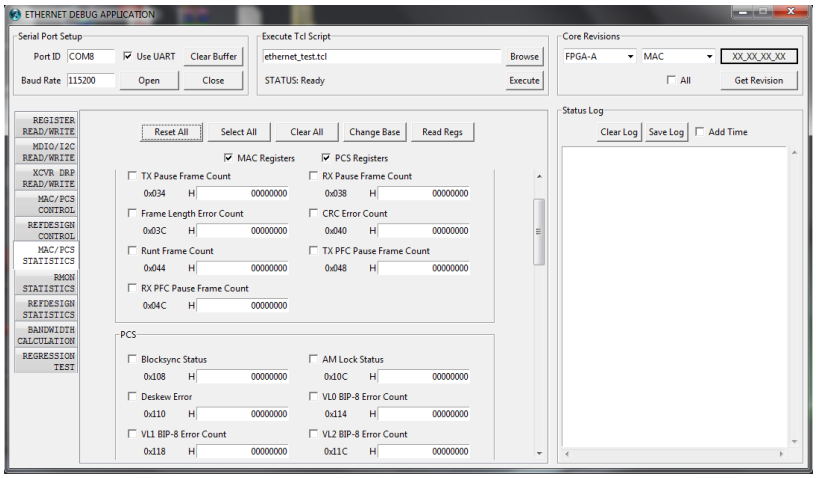
Ethernet Solutions from GiGE to10Gbps: HTG-K7-PCIE targeted and fully verified Ethernet interfaces using GiGE, Low Latency and Ultra-Low Latency 10Gbps Ethernet solutions. Ethernet interfaces provided through Hitech Global HTG-FMC-X4SFP+, HTG-FMC-X2QSFP+ and HTG-FMC-SFP-OC FMC modules. Basic L2 packet generators and checkers (netlist) included for quick interface verification through GUI interface.

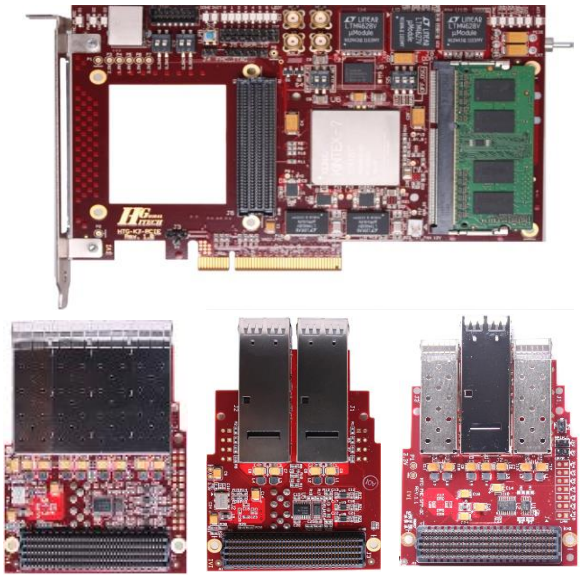
BPI Flash Upgrade through PCIe: Program and erase the parallel Flash memory on the HTG-K7-PCIE through the PCIe interface at very high speeds. Integrating the FUp controller allows any user design to be field upgradable through PCIe.

Device Drivers: 64-bit Linux device drivers in source code for DMA, register access and interrupts

APIs: C (source code) language function libraries and example test for DMA, register access and interrupts in source code

GUI Interface: GUI application (Linux only) for control and configuration of all EFW components





Links to IP Core and Module Resources

- 40G Ethernet IP http://www.hitechglobal.com/IPCores/40Gig_EthernetMAC.htm
- 10G Low-Latency Ethernet IP: http://www.hitechglobal.com/IPCores/10GigEMAC.htm
- DMA Controller IP:

For more information:

Phone: +1-408-781-8043

Email: info@hitechglobal.com

Product Ordering Codes

Base (No Ethernet/DMA):	**HTK-EFW-K7-PCIe-Base**
GiGe Ethernet:	**HTK-EFW-K7-PCIe-1G**
Low Latency 10G Ethernet:	**HTK-EFW-K7-PCIe-10G**
Ultra-Low Latency 10G:	**HTK-EFW-K7-PCIe-10GU**