# Extensible FPGA Framework (EFW)
# For HiTech Global HTG-830 Kintex-Ultrascale PCIe FPGA Module

## Key Framework Features

- Integrated, hardware verified solutions for 1G/10G/40G Ethernet development
- HTG-830 module targeted system building blocks of DMA Controllers, Ethernet MAC and PCS, PCIe application interface, AXI4 Interconnect, DDR4 and Flash Memory controllers
- Frameworks bundled with:
  - ***All options:*** x4/x8 PCIe Gen3 PCIe application interface, AXI4-Lite master/arbiter for memory mapped interface, Field Upgradeable (FUp) controller for in-system Flash programming and I2C controller
  - ***Selected Option Based:*** Synthesizable binaries and full simulation libraries for GiGE, Low Latency 10G, Ultra-Low Latency 10G, Extreme-Low Latency 10G or 40G Ethernet
- Linux source code device drivers and APIs for PCIe interface and DMA controller
- Unified GUI for the entire EFW with scripting support
- Lowest startup cost for developing complete 1G, 10G and 40G solutions with Kintex Ultrascale FPGA
- Simplified, single-sourced licensing for all FPGA IP cores and drivers

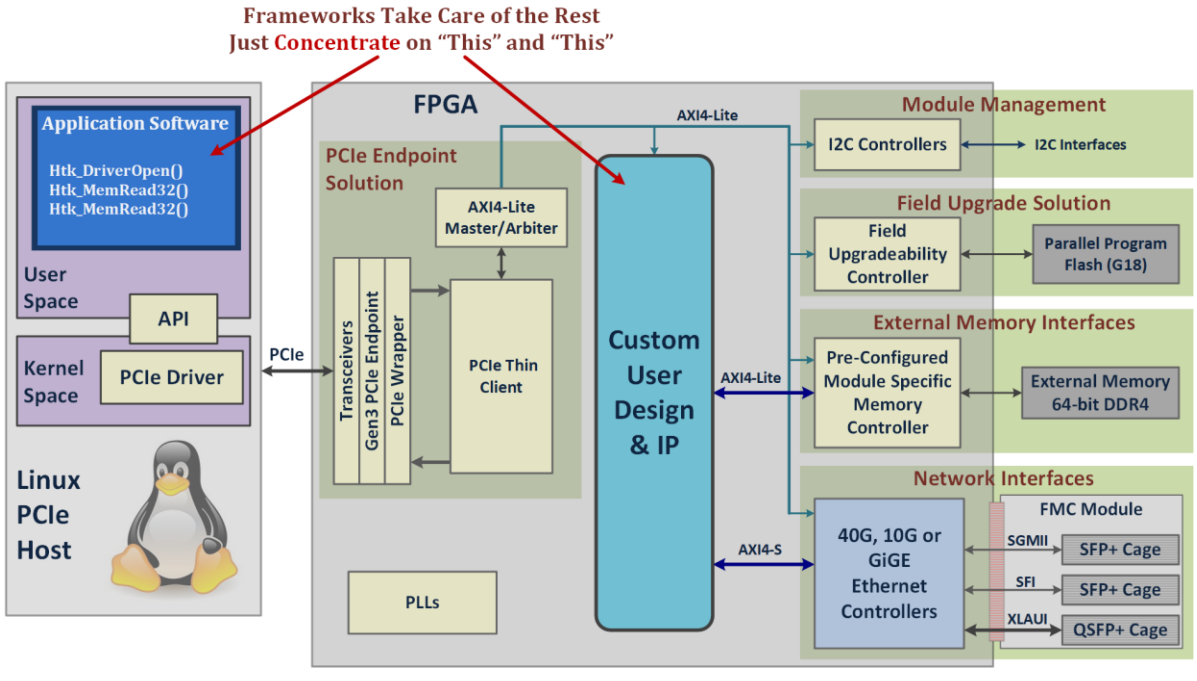
## QUICKEST AND HIGHLY AFFORDABLE 1G, 10G AND 40G ETHERNET DEVELOPMENT WITH HTG-830 PCIe MODULE

Extensible FPGA Framework (EFW) empowers FPGA developers with a verified set of productivity solutions, including module targeted physical interface components, device drivers and APIs for the HiTech Global HTG-830 PCIe module.

Frameworks save months of development and debug time by enabling developers to skip the tedious and time-consuming phase of IP core integration, interface verification and firmware development.

| *Framework Bundled Content* | *Framework Type* | | | | *Required FMC Module* |
|---|---|---|---|---|---|
| | *Base* | *1G* | *10G* | *40G* | |
| Linux Device Drivers and APIs (Source) | ● | ● | ● | ● | - |
| x8 Gen3 PCIe hard IP based PCIe Endpoint Wrapper (Verilog) | ● | ● | ● | ● | - |
| PCIe Thin Client for Memory Mapped Access (Netlist) | ● | ● | ● | ● | - |
| AXI4-Lite Master and Arbiter with 32-bit control plane for registers accesses (Verilog) | ● | ● | ● | ● | - |
| 32-bit AXI4-Lite Slave for integrating user blocks (Verilog) | ● | ● | ● | ● | - |
| G18 Flash controller for in-system field upgrades (FuP) (Netlist) | ● | ● | ● | ● | - |
| I2C Controllers (Netlist) | ● | ● | ● | ● | - |
| SPI Controller (Verilog) | ● | ● | ● | ● | - |
| Targeted DDR4 controllers with AXI4 wrapper (Verilog) | ● | ● | ● | ● | - |
| GiGE MAC with 1000Base-X Interface (Netlist) | | ● | ● | ● | FMC-X4SFP+ |
| Low, Ultra-Low and Extreme-Low Latency 10G Ethernet option (Netlist) ***Latency optimized for financial market applications*** | | | ● | | FMC-X4SFP+ FMC-SFP-OC |
| 40G Ethernet, 128-bit data path (Netlist) ***Area optimized for low resource utilization*** | | | | ● | FMC-X2QSFP+ FMC-SFP-OC |

** GiGE, 10G and 40G UDP/IP Offload Engine (UOE) IP cores also available*



## Productivity Features

***PCIe Bus Interface and Management:*** Complete PCIe solutions for the HTG-830 x8 Gen3 PCIe interface. Framework implements a 32-bit AXI4-Lite compliant register access interface for Non-DMA (single read/write) operations.
***Parameterized AXI4-Lite Inter-connect:*** Complete, fully parameterized 32-bit AXI4-Lite inter-connect with Master, Arbiter and Slave in source (Verilog) code for register access.

***Ethernet Solutions from GiGE to 40Gbps:*** HTG-830 targeted and fully verified Ethernet interfaces using GiGE, Optimal Latency 10Gbps and 40Gbps Ethernet solutions. Ethernet interfaces provided through Hitech Global HTG-FMC-X4SFP+, HTG-FMC-X2QSFP+ and HTG-FMC-SFP-OC FMC modules. Basic L2 packet generators and checkers (netlist) included for quick interface verification through GUI interface. GiGE, 10Gbps and 40Gbps UDP/IP Offload Engine (UOE) IP cores also available for hardware protocol acceleration.

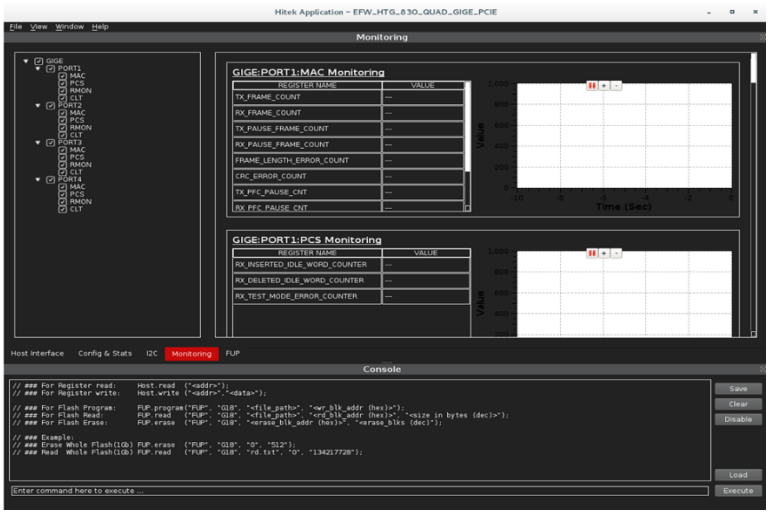
***BPI Flash Upgrade through PCIe:*** Program and erase the parallel Flash memory on the HTG-830 through the PCIe interface at very high speeds. Integrating the FUp controller allows any user design to be field upgradable through PCIe.

***I2C and SPI Controllers:*** Flexible I2C and SPI controllers with AXI4-Lite host interface for peripheral device management.

***Device Drivers:*** 64-bit Linux device drivers in source code register access and interrupts.

***APIs:*** C (source code) language function libraries and example test for register access and interrupts in source code.

***GUI Interface:*** GUI application (Linux only) for control and configuration of all EFW components.




## Links to IP Core and Module Resources

- 40G Ethernet IP: http://www.hitechglobal.com/IPCores/40Gig_EthernetMAC.htm
- 10G Low Latency Ethernet IP: http://www.hitechglobal.com/IPCores/10GigEMAC.htm
- 10G Ultra-Low Latency Ethernet IP: http://www.hitechglobal.com/IPCores/
- 10G Extreme-Low Latency Ethernet IP: http://www.hitechglobal.com/IPCores/Extreme_Low_Latency_10G_Ethernet.htm

For more information:
*Phone:* +1-408-781-8043
*Email:* info@hitechglobal.com

***Product Ordering Codes***

| | |
|---|---|
| **Base (No Ethernet):** | **HTK-EFW-830-Base** |
| **GiGe Ethernet:** | **HTK-EFW-830-1G** |
| **Low Latency 10G Ethernet:** | **HTK-EFW-830-10G** |
| **Ultra-Low Latency 10G:** | **HTK-EFW-830-10GU** |
| **Extreme-Low Latency 10G:** | **HTK-EFW-830-10GEx** |
| **40G Ethernet:** | **HTK-EFW-830-40G** |