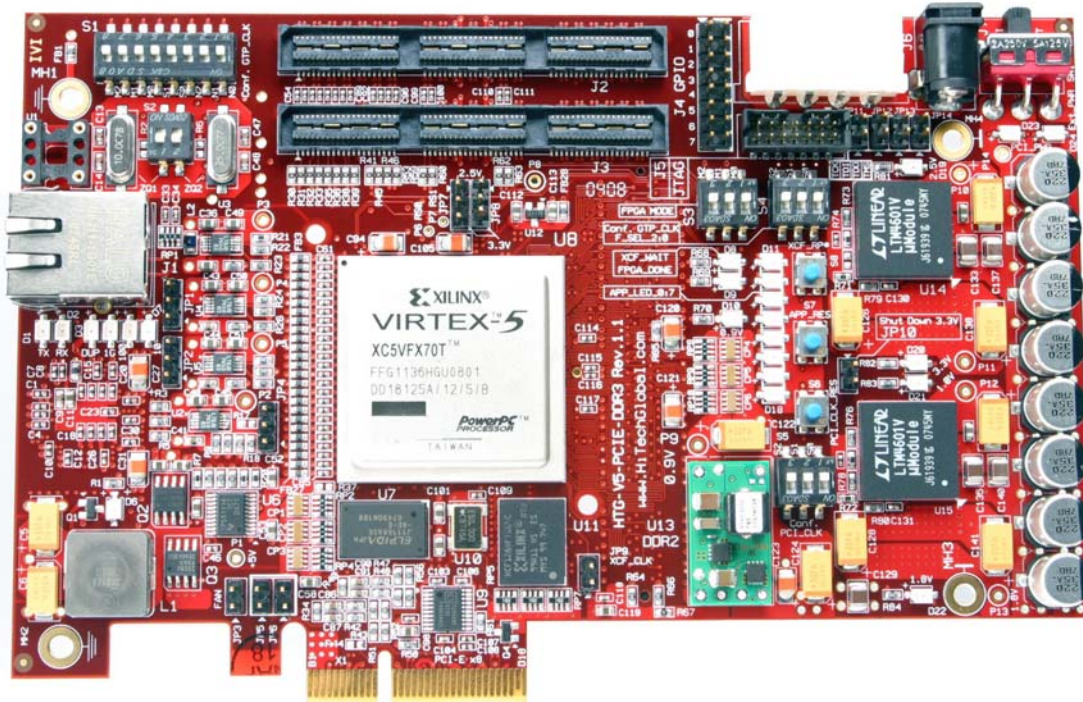




HiTech Global Virtex™-5 FXT/LXT/SXT Development Platform for PCI Express® Generation 1 & 2

HTG-V5-PCIE2 User Manual

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DDR-2 DDR-3 PowerPC 440 DSP

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Date	Version	Notes
12/01/2007	1.0	
2/29/2008	1.1	Platform Flash configuration info added
5/1/2008	1.2	FXT info added
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Table Of Contents

Chapter 1: Introduction to Virtex-5

- 1.1) Virtex-5 FPGA General Description
- 1.2) Summary of Features
- 1.3) Supported Virtex-5 Devices
- 1.4) RocketIO/O Multi Gigabit Transceivers (GTP/GTX)
- 1.5) End-Point Block for PCI Express
- 1.6) PowerPC 440 RISC Cores (FXT Only)
- 1.7) Tri-Mode Ethernet MAC
- 1.8) Input/Output Blocks (SelectIOs)
- 1.9) Additional Virtex-5 Resources

Chapter 2: Virtex-5 FPGA Platform for PCI Express

- 2.1) Introduction
- 2.2) Kit Content
- 2.3) System Requirements
- 2.4) Summary Of Features
- 2.5) Board Setup
- 2.6) Block Diagram
- 2.7) User I/O Resource Distribution & Clocks
- 2.8) PCI Express
- 2.9) High Speed IOs (Single-Ended/LVDS & Data-Rate-Adjustable RocketIO GTP/GTX Transceivers)
- 2.10) DDR 2 Memory (SODIMM)
- 2.11) DDR 3 Memory (Component)
- 2.12) 10/100/1000 Gigabit Ethernet
- 2.13) User LEDs and Switches
- 2.14) Configuration

Chapter 3: Accessories

- 3.1) Communication Module
- 3.2) CX4/SMA Module
- 3.3) High-Speed Cable
- 3.4) Customized PC

Chapter 4: PCI Express Software & Drivers

- 4.1) Introduction
- 4.2) Overview
- 4.3) Architecture and Operation
- 4.4) Build Instructions

Chapter 4: Intellectual Property (IP) Cores

- 5.1) PCI Express
- 5.2) DDR 2 Memory Controller
- 5.3) DDR 3 Memory Controller

Chapter 1: Introduction to Virtex-5

1.1) Virtex-5 FPGA

The Virtex-5 family provides the newest most powerful features in the FPGA market. Using the second generation ASMBL™ (Advanced Silicon Modular Block) column-based architecture, the Virtex-5 family contains four distinct platforms (sub-families), the most choice offered by any FPGA family. Each platform contains a different ratio of features to address the needs of a wide variety of advanced logic designs. In addition to the most advanced, high-performance logic fabric, Virtex-5 FPGAs contain many hard-IP system level blocks, including powerful 36-Kbit block RAM/FIFOs, second generation 25 x 18 DSP slices, SelectIO™ technology with built-in digitally controlled impedance, ChipSync™ source-synchronous interface blocks, system monitor functionality, enhanced clock management tiles with integrated DCM (Digital Clock Managers) and phase-locked-loop (PLL) clock generators, and advanced configuration options.

Additional platform dependant features include power-optimized high-speed serial transceiver blocks for enhanced serial connectivity, integrated Endpoint blocks for PCI Express, tri-mode Ethernet MACs (Media Access Controllers), and high-performance PowerPC® 440 microprocessor embedded blocks. These features allow advanced logic designers to build the highest levels of performance and functionality into their FPGA-based systems. Built on a 65-nm state-of-the-art copper process technology, Virtex-5 FPGAs are a programmable alternative to custom ASIC technology. Most advanced system designs require the programmable strength of FPGAs. Virtex-5 FPGAs offer the best solution for addressing the needs of high-performance logic designers, high-performance DSP designers, and high-performance embedded systems designers with unprecedented logic, DSP, hard/soft microprocessor, and connectivity capabilities. The Virtex-5 LXT, SXT, and FXT platforms include advanced high-speed serial connectivity and link/transaction layer capability.

1.2) Summary of Features

- Four platforms LX, LXT, SXT, and FXT
 - Virtex-5 LX: High-performance general logic applications
 - Virtex-5 **LXT**: High-performance logic with advanced serial connectivity
 - Virtex-5 **SXT**: High-performance signal processing applications with advanced serial connectivity
 - Virtex-5 **FXT**: High-performance embedded systems with advanced serial connectivity
- Cross-platform compatibility
 - LXT, SXT, and FXT devices are footprint compatible in the same package using adjustable voltage regulators
- Most advanced, high-performance, optimal-utilization, FPGA fabric
 - Real 6-input look-up table (LUT) technology
 - Dual 5-LUT option
 - Improved reduced-hop routing
 - 64-bit distributed RAM option
 - SRL32/Dual SRL16 option
- Powerful clock management tile (CMT) clocking
 - Digital Clock Manager (DCM) blocks for zero delay buffering, frequency synthesis, and clock phase shifting
 - PLL blocks for input jitter filtering, zero delay buffering, frequency synthesis, and phase-matched clock division
- 36-Kbit block RAM/FIFOs
 - True dual-port RAM blocks
 - Enhanced optional programmable FIFO logic
 - Programmable

- True dual-port widths up to x36
- Simple dual-port widths up to x72
 - Built-in optional error-correction circuitry
 - Optionally program each block as two independent 18- Kbit blocks
- High-performance parallel SelectIO technology
 - 1.2 to 3.3V I/O Operation
 - Source-synchronous interfacing using ChipSync™ technology
 - Digitally-controlled impedance (DCI) active termination
 - Flexible fine-grained I/O banking
 - High-speed memory interface support
- Advanced DSP48E slices
 - 25 x 18, two's complement, multiplication
 - Optional adder, subtracter, and accumulator
 - Optional pipelining
 - Optional bitwise logical functionality
 - Dedicated cascade connections
- Flexible configuration options
 - SPI and Parallel FLASH interface
 - Multi-bitstream support with dedicated fallback reconfiguration logic
 - Auto bus width detection capability
- System Monitoring capability on all devices
 - On-chip/Off-chip thermal monitoring
 - On-chip/Off-chip power supply monitoring
 - JTAG access to all monitored quantities
- Integrated Endpoint blocks for PCI Express
 - LXT, SXT, and FXT Platforms
 - Compliant with the PCI Express Base Specification 1.1
 - x1, x4, or x8 lane support per block
 - Works in conjunction with RocketIO™ transceivers
- Tri-mode 10/100/1000 Mb/s Ethernet MACs
 - LXT, SXT, and FXT Platforms
 - RocketIO transceivers can be used as PHY or connect to external PHY using many soft MII (Media Independent Interface) options
- RocketIO™ GTP transceivers 100 Mb/s to 3.75 Gb/s
 - LXT and SXT Platforms
- RocketIO GTX transceivers 150 Mb/s to 6.5 Gb/s
 - FXT Platform only
- PowerPC 440 Microprocessors
 - FXT Platform only
 - RISC architecture
 - 7-stage pipeline
 - 32-Kbyte instruction and data caches included
 - Optimized processor interface structure (crossbar)
- 65-nm copper CMOS process technology
- 1.0V core voltage
- High signal-integrity flip-chip packaging available in standard

1.3) Supported Virtex-5 Devices

Part Number	LX50T	LX85T	LX110T	LX155T	SX50T	SX95T	FX70T	FX100T
Slices	7,200	12,960	17,280	24,320	8,160	14,720	11,200	16,000
Logic Cells	46,080	82,944	110,592	155,648	52,224	94,208	71,680	102,400
CLB Flip-Flops	28,800	51,840	69,120	97,280	32,640	58,880	44,800	64,000
Maximum Distributed RAM (Kbits)	480	840	1,120	1,640	780	1,520	820	1,240
Block RAM/FIFO w/ECC (36Kbits each)	60	108	148	212	132	244	148	228
Total Block RAM (Kbits)	2,160	3,888	5,328	7,632	4,752	8,784	5,328	8,208
Digital Clock Managers (DCM)	12	12	12	12	12	12	12	12
Phase Locked Loop (PLL)/PMCD	6	6	6	6	6	6	6	6
Maximum Single-Ended Pins	480	480	680	680	480	640	640	680
Maximum Differential I/O Pairs	240	240	340	340	240	320	320	340
DSP48E Slices	48	48	64	128	288	640	128	256
PowerPC® 440 Processor Blocks	—	—	—	—	—	—	1	2
Integrated Endpoint Blocks for PCI Express	1	1	1	1	1	1	3	3
10/100/1000 Ethernet MAC Blocks	4	4	4	4	4	4	4	4
RocketIO™ GTP Low-Power Transceivers	12	12	16	16	12	16	—	—
RocketIO™ GTX High-Power Transceivers	—	—	—	—	—	—	16	16
Commercial	-1, -2, -3	-1, -2, -3	-1, -2, -3	-1, -2, -3	-1, -2, -3	-1, -2	-1, -2, -3	-1, -2, -3
Industrial	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2
Configuration Memory (Mbits)	14.1	23.3	31.1	43	20	35.7	27	39.4

Table (1): Supported Virtex-5 Devices

1.4) RocketIO Multi Gigabit Serial Transceivers

GTP Transceivers (LXT/SXT only)

- Full-duplex serial transceiver capable of 100 Mb/s to 3.75 Gb/s baud rates
- 8B/10B, user-defined FPGA logic, or no encoding options
- Channel bonding support
- CRC generation and checking
- Programmable pre-emphasis or pre-equalization for the transmitter
- Programmable termination and voltage swing
- Programmable equalization for the receiver
- Receiver signal detect and loss of signal indicator
- User dynamic reconfiguration using secondary configuration bus
- Out of Band (OOB) support for Serial ATA (SATA)
- Electrical idle, beaconing, receiver detection, and PCI Express and SATA spread-spectrum clocking support
- Less than 100 mW typical power consumption
- Built-in PRBS Generators and Checkers

GTX Transceivers (FXT Only)

- Full-duplex serial transceiver capable of 150 Mb/s to 6.5 Gb/s baud rates
- 8B/10B encoding and programmable gearbox to support 64B/66B and 64B/67B encoding, user-defined FPGA logic, or no encoding options
- Channel bonding support
- CRC generation and checking
- Programmable pre-emphasis or pre-equalization for the transmitter
- Programmable termination and voltage swing
- Programmable continuous time equalization for the receiver

- Programmable decision feedback equalization for the receiver
- Receiver signal detect and loss of signal indicator
- User dynamic reconfiguration using secondary configuration bus
- OOB support (SATA)
- Electrical idle, beaconing, receiver detection, and PCI Express spread-spectrum clocking support
- Low-power operation at all line rates

1.5) Integrated Endpoint Block for PCI Express

- Works in conjunction with RocketIO GTP transceivers (LXT and SXT) and GTX transceivers (FXT) to deliver full PCI Express Endpoint functionality with minimal FPGA logic utilization.
- Conforms to the PCI Express Base Specification 1.1
- PCI Express Endpoint block or Legacy PCI Express Endpoint block
- x8, x4, x2, or x1 lane width
- Power management support
- Block RAMs used for buffering
- Fully buffered transmit and receive
- Management interface to access PCIe configuration space and internal configuration
- Support for a wide range of maximum payload size (up to 512Bytes with the Block Plus Wrapper)
- One virtual channel (VCs)
- Up to 6 x 32 bit or 3 x 64 bit BARs (or a combination of 32 bit and 64 bit)

1.6) PowerPC 440 RISC Cores (FXT Only)

- Embedded PowerPC 440 (PPC440) cores
 - Up to 550 MHz operation
 - Greater than 1000 DMIPS per core
 - Seven-stage pipeline
 - Multiple instructions per cycle
 - Out-of-order execution
 - 32 Kbyte, 64-way set associative level 1 instruction cache
 - 32 Kbyte, 64-way set associative level 1 data cache
 - Book E compliant
- Integrated crossbar for enhanced system performance
 - 128-bit Processor Local Buses (PLBs)
 - Integrated scatter/gather DMA controllers
 - Dedicated interface for connection to DDR2 memory controller
 - Auto-synchronization for non-integer PLB-to-CPU clock ratios
- Auxiliary Processor Unit (APU) Interface and Controller
 - Direct connection from PPC440 embedded block to FPGA fabric-based coprocessors
 - 128-bit wide pipelined APU Load/Store
 - Support of autonomous instructions: no pipeline stalls
 - Programmable decode for custom instructions

1.7) Tri-Mode (10/100/1000 Mb/s) Ethernet Media Access Control (MAC)

Virtex-5 FXT/LXT/SXT devices contain four embedded Ethernet MAC blocks. The blocks have the following characteristics:

- IEEE 802.3 compliant
- UNH-compliance tested
- MII/GMII Interface with SelectIO or SGMII interface when used with RocketIO transceivers
- Half or full duplex
- Supports Jumbo frames
- 1000 Base-X PCS/PMA: When used with RocketIO GTP transceiver, can provide complete 1000 Base-X implementation on-chip
- DCR-bus connection to microprocessors

1.8 Input/Output Blocks (SelectIOs)

IOBs are programmable and can be categorized as follows:

- Programmable single-ended or differential (LVDS) operation
- Input block with an optional single data rate (SDR) or double data rate (DDR) register
- Output block with an optional SDR or DDR register
- Bidirectional block
- Per-bit deskew circuitry
- Dedicated I/O and regional clocking resources
- Built in data serializer/deserializer The IOB registers are either edge-triggered D-type flip-flops or level-sensitive latches.

IOBs support the following single-ended standards:

- LVTTTL
- LVCMOS (3.3V, 2.5V, 1.8V, 1.5V, and 1.2V)
- PCI (33 and 66 MHz)
- PCI-X
- GTL and GTLP
- HSTL 1.5V and 1.8V (Class I, II, III, and IV)
- HSTL 1.2V (Class 1)
- SSTL 1.8V and 2.5V (Class I and II)

The Digitally Controlled Impedance (DCI) I/O feature can be configured to provide on-chip termination for each single-ended I/O standard and some differential I/O standards.

The IOB elements also support the following differential signaling I/O standards:

- LVDS and Extended LVDS (2.5V only)
- BLVDS (Bus LVDS)
- ULVDS
- Hypertransport™
- Differential HSTL 1.5V and 1.8V (Class I and II)
- Differential SSTL 1.8V and 2.5V (Class I and II)
- RSDS (2.5V point-to-point)

Two adjacent pads are used for each differential pair. Two or four IOB blocks connect to one switch matrix to access the routing resources. Per-bit deskew circuitry allows for programmable signal delay internal to the FPGA. Per-bit deskew flexibly provides fine-grained increments of delay to carefully produce a range of signal delays. This is especially useful for synchronizing signal edges in source-synchronous interfaces.

General purpose I/Os in select locations (eight per bank) are designed to be “regional clock capable” I/O by adding special hardware connections for I/O in the same locality. These regional clock inputs are distributed within a limited region to minimize clock skew between IOBs. Regional I/O clocking supplements the global clocking resources.

1.9) Additional Virtex 5 information and documents are available at the following sites:**Virtex-5 User Guide**

http://www.xilinx.com/support/documentation/user_guides/ug190.pdf The Virtex™-5 User Guide includes chapters on Clocking Resources, Clock Management Technology, Phase-Locked Loops, Block RAM and FIFO memory, Configurable Logic Blocks (CLBs), SelectIO resources, and SelectIO™ logic resources.

Virtex-5 XtremeDSP User Guide http://www.xilinx.com/support/documentation/user_guides/ug193.pdf

This document describes the Virtex-5 DSP48E slice.

Virtex-5 Configuration User Guide

http://www.xilinx.com/support/documentation/user_guides/ug191.pdf This all-encompassing configuration guide includes detailed information on the Virtex™-5 configuration interfaces (JTAG, Serial, SelectMAP, SPI and BPI), and it discusses flows and techniques for bitstream encryption, readback and reconfiguration.

Virtex-5 Packaging and Pinout Specification

http://www.xilinx.com/support/documentation/user_guides/ug195.pdf This user guides describes Virtex™-5 device pinouts and package specifications, and pinout diagrams and thermal data.

Virtex-5 RocketIO GTP Transceiver User Guide

http://www.xilinx.com/support/documentation/user_guides/ug196.pdf This guide describes the RocketIO™ GTP transceivers available in the Virtex-5 LXT platform devices.

Virtex-5 RocketIO GTX Transceiver User Guide

http://www.xilinx.com/support/documentation/user_guides/ug198.pdf

This guide describes the RocketIO™ GTX transceivers available in the Virtex-5 FXT platform devices.

LogiCORE IP Endpoint Block Plus for PCI Express User Guide

http://www.xilinx.com/support/documentation/ip_documentation/pcie_blk_plus_ug341.pdf

This guide describes the functionality of the Endpoint Block Plus wrapper for PCI Express using the Integrated Endpoint Block for PCI Express available in the Virtex-5 LXT/SXT/FXT devices.

Virtex-5 Embedded Tri-Mode Ethernet MAC User Guide

http://www.xilinx.com/support/documentation/user_guides/ug194.pdf This guide describes the dedicated Tri-Mode Ethernet Media Access Controller (MAC) available in the Virtex™-5 LXT platform devices.

Virtex-5 System Monitor User Guide

http://www.xilinx.com/support/documentation/user_guides/ug192.pdf This guide describes the System Monitor functionality available in all Virtex™-5 devices.

Virtex-5 PCB Designer's Guide http://www.xilinx.com/support/documentation/user_guides/ug203.pdf This guide provides information on PCB design for Virtex™-5 devices, with a focus on strategies for making design decisions at the PCB and interface level.

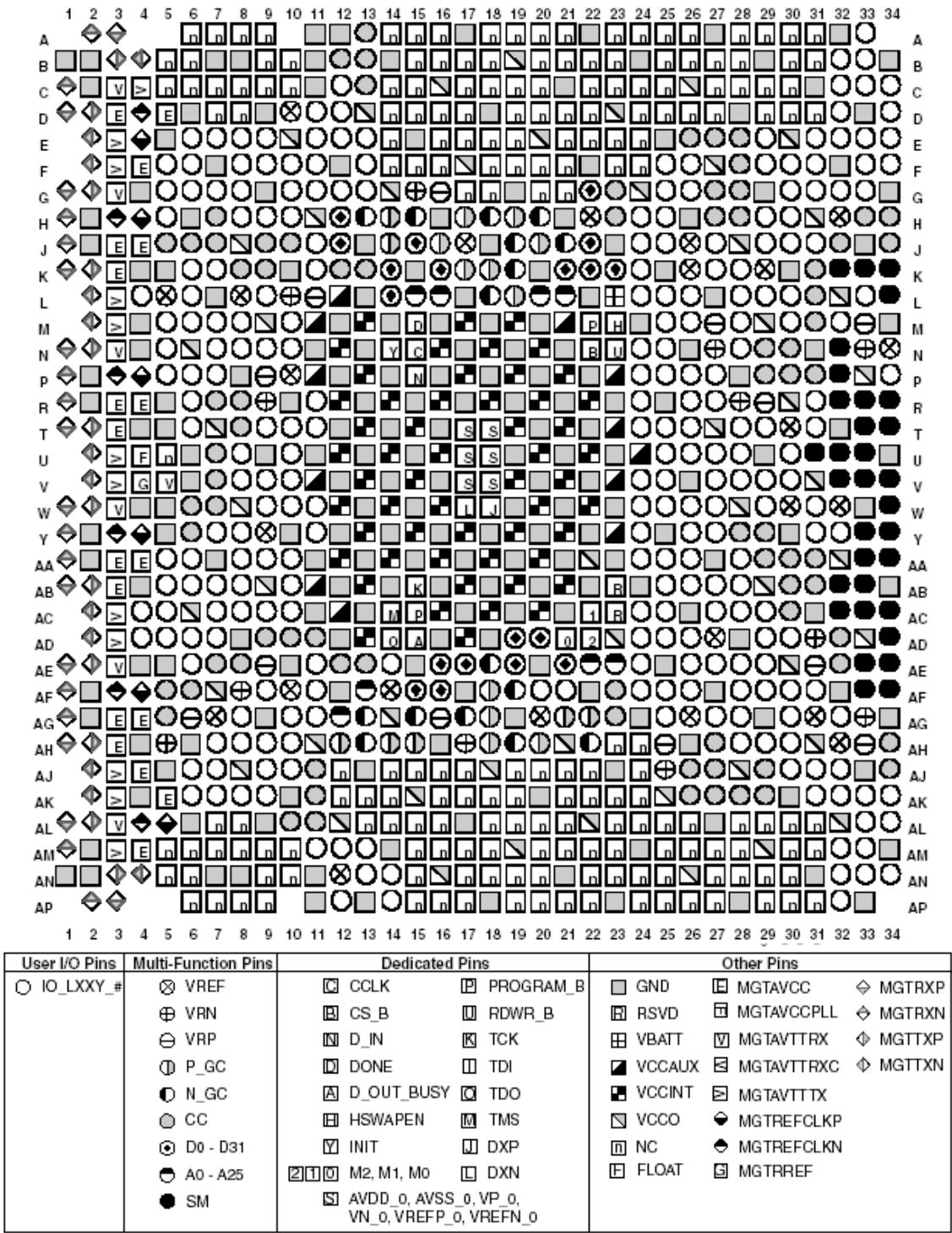


Figure (1): Virtex-5 FF1136 Package

Chapter 2: Virtex-5 FPGA Platform for PCI Express

2.1) Introduction

The V5-PCIE2 board series are powered by Xilinx Virtex-5 FX70T, FX100T, LX110T, LX155T or SX95T FPGA devices (with FF1136 footprint). The FXT models can be used for both PCI Express Gen 1 & 2 (using hard macro PCIe controller for Gen 1 and soft IP core for Gen2). The LXT/SXT models can only be used for PCI Express Gen 1 applications.

The V5-PCIE2 series provide wide variety of connectors and interfaces including ;one x4 PCI Express edge connector , one Gigabit Ethernet (10/100/1000), eight rate-adjustable RocketIO GTP/GTX ports with super clock, and 50 pairs of LVDS IOs (for any customized or off-the-shelf modules such as FPGA expansion, DVI, USB, etc.)

The V5-PCIE2 boards provide access to up to 4 GB of DDR-2 (through one set of SO-DIMM socket) and 1 Mb of DDR-3 memory (component).

The V5-PCIE2 boards can be used either as a stand-alone development board or PCI Express add-in card. This provides additional functionality and cost saving so designers can use the board for multiple designs and projects. Switch SW1 can be used for switching between PCI Express and Stand-alone modes.

PCI Express Mode: → **SW1 ON** (when board is plugged into a PCI Express slot and powered by the 12V supply from motherboard)

Stand-alone Mode: → **SW1 OFF** (when board is in stand alone mode and powered by an external 5V supply)

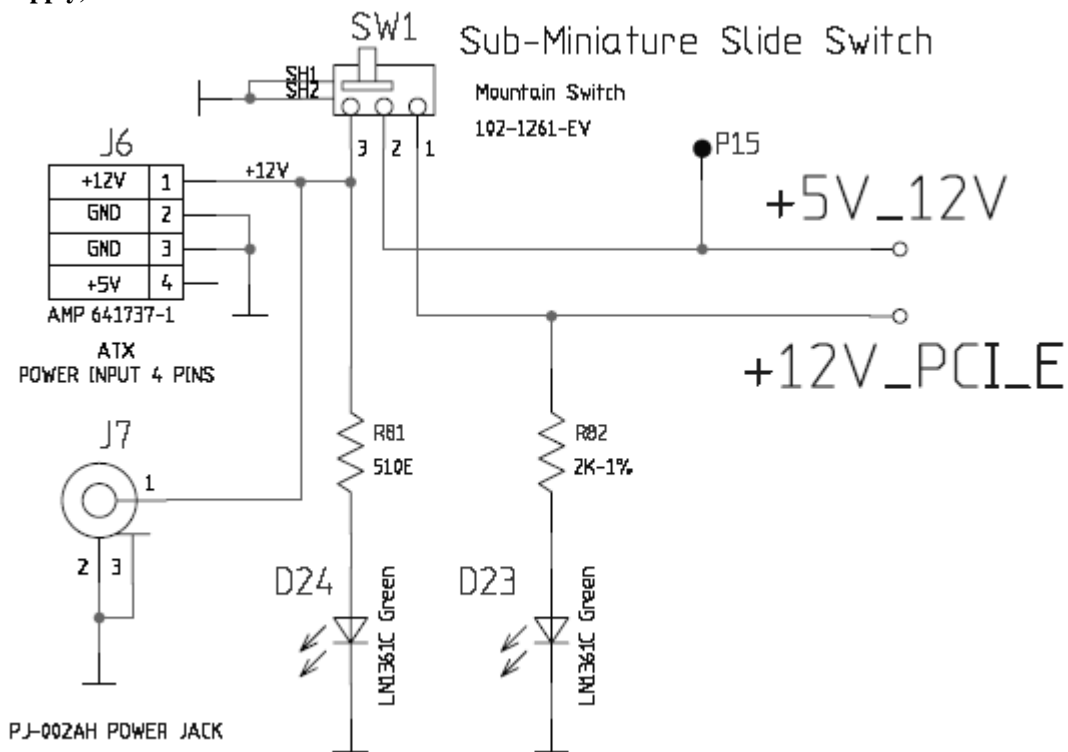


Figure (2) : Operation Mode Select (PCI Express vs. Stand-Alone)

The feature-rich Virtex-5 devices, availability of more than 100 different **IP Cores** through HiTech Global, and a variety of different connectors and interfaces, make the V5-PCIE2 an extremely versatile platform for serial interface, embedded system, and storage designs. A complete list of IP Cores supported by HiTech Global is available at <http://www.hitechglobal.com/ipcores/>

The Virtex-5 V5-PCIE2 can be bundled and shipped with the following IP Cores:

- DDR 2 Memory Controller <http://www.hitechglobal.com/IPCores/DDR2Controller.htm>
- DDR 3 Memory Controller <http://www.hitechglobal.com/IPCores/DDR3Controller.htm>
- PCI Express Back-End (Provides a high-performance DMA Engine and a simplified user interface)

2.2) Kit Content

- The Virtex- 5 HTG-V5-PCIE2 PCI Express Board
- FX100T/FX70T (Gen 2), SX95T/LX110T/LX155T (Gen 1)
- Jungo WinDriver™ Software Drivers for Linux and Windows (30-day Evaluation) – Also available at: <http://www.jungo.com/st/partners/hitechglobal.html>
- CD-ROM
 - Schematics (searchable .pdf), User Manual, PCIe Gen 1 or 2 Reference Designs (in binary format), PCIe Graphic User Interface (GUI), User Constraint Files (UCF), Xilinx Board Definition (XBD) files, Gerber Data (Top & Bottom), etc.
- PCIe Bracket
- 512 MB DDR-2 SO-DIMM

2.3) System Requirements

- Hardware:
 - PC or Server with PCI Express Gen 1 and/or 2 slot . The following PC Mother board with multiple PCIe slots is available through HiTech Global:
(http://www.hitechglobal.com/Accessories/PCIExpress-Gen2_PC.htm)
 - X4 boards can be plugged into x8 slots
 - X4 boards can be plugged into x1 slots via an adapter
 - Xilinx USB Programming Cable (HW-USB-G)
- Software Tools
 - Xilinx ISE™ Foundation 10.1 (EF-ISE-FND)
 - PCI Express Driver and GUI (provided)
 - EDK for embedded sys. Development (EF-EDK)
 - ChipScope Pro™ & Serial IO Tool Kit for debugging (EF-CSP-PRO)

2.4) Summary of Features:

- Xilinx Virtex-5 LXT/SXT/FXT in FF1136 package
- Xilinx 128Mb Platform Flash XL for configuration and user flash
- 4-Lane PCI Express End-Point Connector (upstream)
- 8 data-rate-adjustable RocketIO GTX/GTP transceivers with Super Clock (J3 connector)
- One Tri Mode Ethernet Connector (10/100/1000)
- 512 Mb of DDR-3 Memory (component)
- One DDR2 SO-DIMM Socket (Up to 4 GB)
- Two LVDS Headers (total of 50 pairs)
- GTP/GTX Super Clock
- User Super Clock
- Adjustable PCI Express Jitter Attenuator
- GTP/GTX, User, and Super Clock Switches

2.5) Board Setup

DIP Switch

S1: Super clock M, N, crystal select (default = all OFF) – Table (5) & (6)

S2: Super clock onboard crystal select (default = all OFF)

S3: Configuration mode select (default = ON ON OFF) – Table (16)

S4: Super clock output select (default = all OFF) – Table (7)

S5: PCI express clock select (default = FXT: OFF OFF OFF, SXT/LXT: ON OFF ON) – Table (4)

S9: User defined Flash bitstream select (default = all OFF)

Jumpers

JP1 & JP2: Ethernet PHY configuration (default = OFF)

JP3: Fan sully voltage (default = OFF)

JP4: VCCPLL voltage change (FXT = shunt over pin 1 & 2 , LXT/SXT shunt over pin 2 & 3)

JP5 & JP6: PCIe Jitter attenuator chip bypass (default = OFF)

JP7 & JP8: Provide either 2.5V (shunt over pin 1 &2) or 3.3V (shunt over pin 2 &3) for the IOs routed to the Samtec high-speed connectors (with this LVDS or non LVDS signals can be used)

JP9: BPI clock (default = ON)

JP10: DNP

JP11, 12, 13, 14: Configuration via PCIe bus (not useable if the Jtag signals are not activated on the PC mother board).

J15: System clock (default = ON)

2.6) Block Diagram & Dimensions

The V5-PCIE2 board's dimensions is 167.5 mm x 108 mm (6.6" x 4.25"). The board's size is in compliance with the PCI Express Specification and can fit in any PC or Server.

Figure (3) illustrates location of the on-board peripherals.

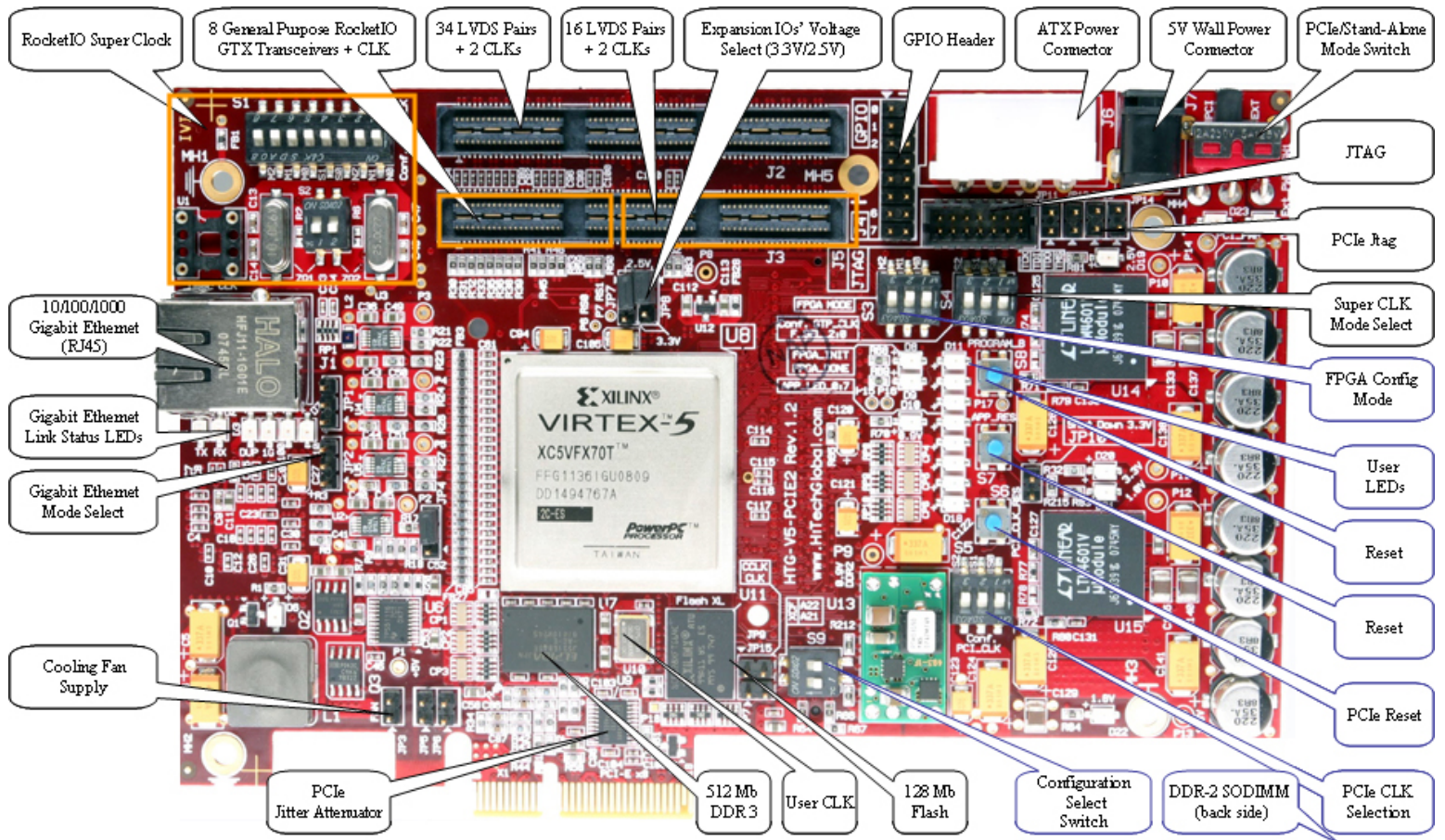


Figure (3): V5-PCIE2 Components Placement

2.7) User I/O Resource Distribution, & Clocking

The on-board Virtex-5 LXT/SXT/FXT FPGA (in FF1136 package) provides total of 480 user I/Os which have been used for connection of different peripherals and components to the FPGA device.

Figure (4.a) illustrates bank distribution for the Rocket and select IOs used by different connectors and peripherals.

Figure (4.b) illustrates clock distribution for different peripherals.

Pg.11 Connector I/O MGT 120	X	X	X	BANK 11 DDR2 SSTL_18 Pg.9
Pg.11 Connector I/O MGT 116	BANK 20 LVDS_25 or LVTTL_33 Pg.12	BANK 3 LVDS_25 or LVTTL_33 Pg.12	BANK 19 LVDS_25 or LVTTL_33 Pg.12	
Pg.5 Connector I/O MGT 112		BANK 1 Boot +3.3V Pg.6	BANK 15 SSTL_18 DDR2	
Pg.5 Connector I/O MGT 114	BANK 18 SSTL_15 DDR3 Pg.7	BANK 0 +3.3V Configuration Pg.6	BANK 17 SSTL_18 DDR2 Pg.9	
Pg.11 PCI-E MGT 118		BANK 2 Boot +3.3V Pg.6	BANK 21 Pg.15 +2.5V Ethernet	
Pg.11 PCI-E MGT 122	X	X	X	
	MGT 124	BANK 5	BANK 23	
	MGT 126	BANK 6	BANK 25	
				BANK 13 DDR2 SSTL_18 Pg.9

Figure (4.a) User I/O Allocation & Distribution

Note: The page numbers are in reference to the schematics

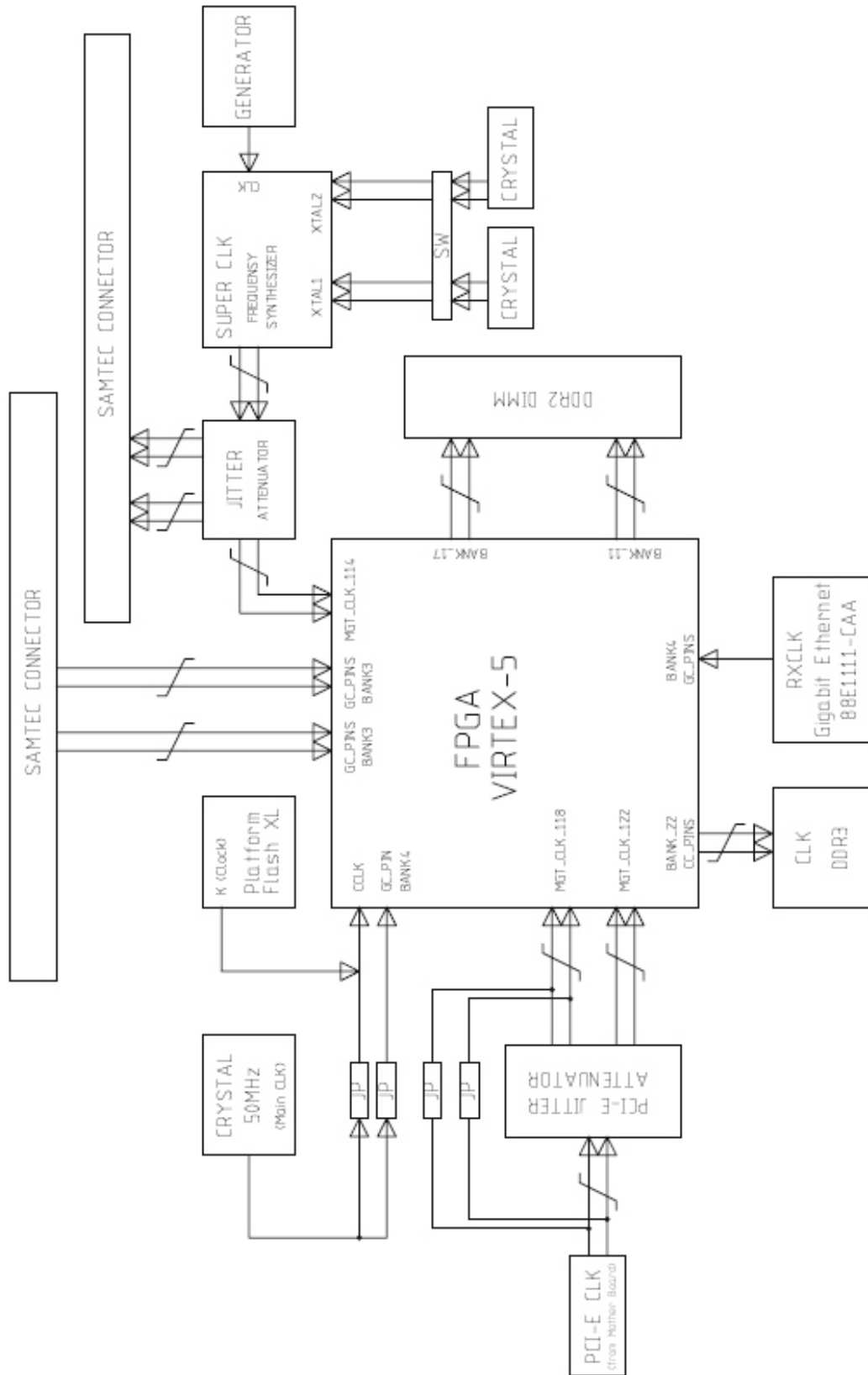
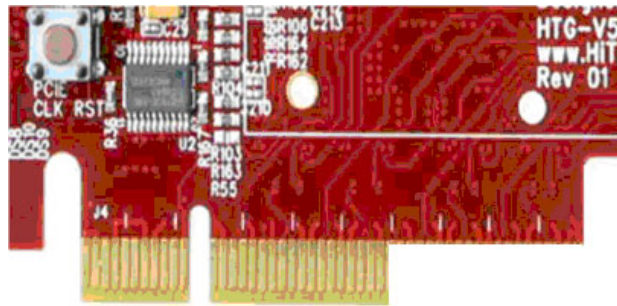


Figure (4.b) Clock Distribution

2.8) PCI Express End Point (Gen 1 & Gen 2)



The Virtex-5 LXT/SXT/FXT FPGA devices provide the Endpoint Block Plus Wrapper for PCI Express to configure the Integrated Endpoint Block for PCI Express Gen 1 and includes additional logic to create a complete Endpoint solution. The Xilinx Endpoint Block Plus Wrapper for PCIe provides many ease-of-use features and optimal configuration for Endpoint applications.

The Endpoint Block Plus Wrapper for PCI is a Xilinx CORE Generator™ IP core, included in the latest IP available through the [Xilinx Download Center](#).

The GTX transceivers in the Virtex-5 FXT FPGA devices used on the V5-PCIE2 platform support PCI Express Gen 2 applications. An additional Soft IP Core for PCI Express Gen2 will be required to instantiate the PCI Express protocol.

HiTech Global provides a complete x4 PCI Express Gen 1 and Gen 2 reference designs with multiple ports DMA engines using either the Endpoint Block Wrapper or the Integrated Endpoint Block for PCI Express (LXT/SXT) or FPGA gates for soft implementation of the PCIe Gen 2. (FXT)

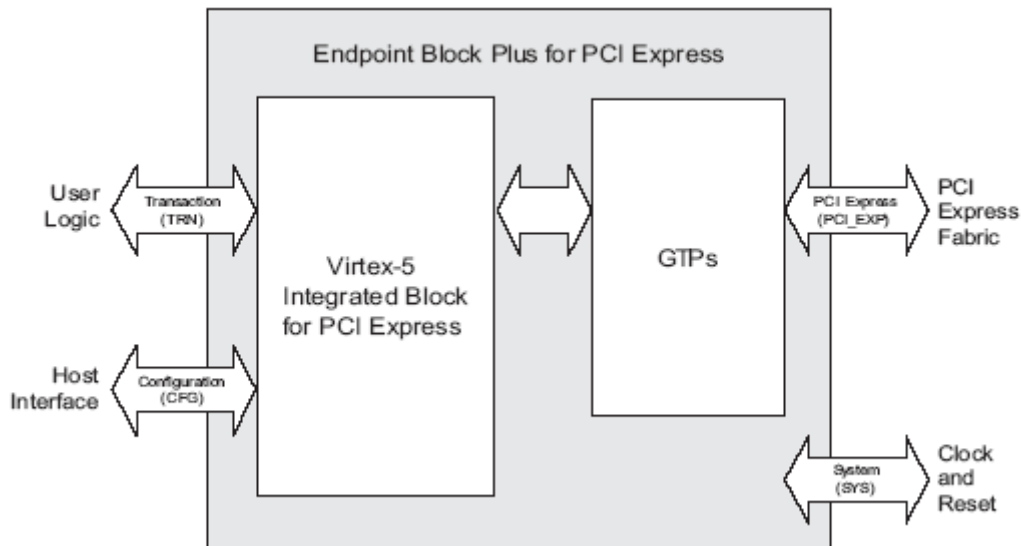


Figure (5) Virtex-5 LXT PCIe Top Level Functional Block and Interfaces

The RocketIO GTP/GTX Transceivers are used along with the Integrated Endpoint Block for PCI express to create a PCI Express Endpoint. The V5-PCIE2 board can be used for PCI Express Gen 1 and Gen 2 x1, x2, and x4 End-Point applications. The PCI Express Edge Connectors can also be used for interfacing to PCI-SIG compliant soft PCI Express IP cores. Contact HiTech Global for availability information regarding soft IP for PCI Express Gen 2.

As illustrated in table (2) and (3), 4 RocketIO GTP/GTX Transceivers are connected to a 4-lane upstream connector for end point applications .

A Side	Signal Name	FPGA Pin #	FPGA Pin Name
A1	PCIE_PRSENT1	AG16	AG16_IO_L7N_GC_VRP_4
A2	+12 VOLTS		
A3	+12 VOLTS		
A4	GND		
A5	JTAG_TCK		
A6	JTAG_TDI		
A7	JTAG_TDO		
A8	JTAG_TMS		
A9	+3.3 VOLTS		
A10	+3.3 VOLTS		
A11	PCIE_PERST	AH17	AH17_IO_L7P_GC_VRP_4
A12	GND		
A13	PCIE_REFCLKP (100 MHz)	AF4, AL5	MGTREFCLKP_118 & 122
A14	PCIE_REFCLKN (100MHz)	AF3, AL4	MGTREFCLKN_118 & 122
A15	GND		
A16	PER0P	AD2	MGTTXP0_118
A17	PER0N	AE2	MGTTXN0_118
A18	GND		
A19	RESERVED		
A20	GND		
A21	PER1P	AJ2	MGTTXP1_118
A22	PER1N	AH2	MGTTXN1_118
A23	GND		
A24	GND		
A25	PER2P	AK2	MGTTXP0_122
A26	PER2N	AL2	MGTTXN0_122
A27	GND		
A28	GND		
A29	PER3P	AN4	MGTTXP1_122
A30	PER3N	AN3	MGTTXN1_122
A31	GND		
A32	RESERVED		

Table (2) PCI Express Upstream Connections Summary -A Side

B Side	Signal Name	FPGA Pin #	FPGA Pin Name
B1	+12 VOLTS		
B2	+12 VOLTS		
B3	+12 VOLTS		
B4	GND		
B5	SMCLK		
B6	SMDAT		
B7	GND		
B8	+3.3 VOLTS		
B9	JTAG_TRST_B		
B10	+3.3 VOLTSAUX		
B11	PCIE_WAKE_B	AF18	AF18_IO_L8P_GC_4
B12	RESERVED		
B13	GND		
B14	PET0P	AE1	MGTRXP0_118
B15	PET0N	AF1	MGTRXN0_118
B16	GND		
B17	PCIE_PRSENT2_B	AG16	AG16_IO_L7N_GC_VRP_4
B18	GND		
B19	PET1P	AH1	MGTRXP1_118
B20	PET1N	AG1	MGTRXN1_118
B21	GND		
B22	GND		
B23	PET2P	AL1	MGTRXP0_122
B24	PET2N	AM1	MGTRXN0_122
B25	GND		
B26	GND		
B27	PET3P	AP3	MGTRXP1_122
B28	PET3N	AP2	MGTRXN1_122
B29	GND		
B30	RESERVED		
B31	PCIE_PRSENT2_B	AG16	AG16_IO_L7N_GC_VRP_4
B32	GND		

Table (3) PCI Express Upstream Connections Summary - B Side

PCI Express Jitter Attenuator

The optional IDT ICS874003-02 is used as PCI Express Jitter Attenuator on the V5-PCIE2 board. This chip is a high performance Differential- to-LVDS Jitter Attenuator designed for use in PCI Express systems. In some PCI Express systems, such as those found in desktop PCs, the PCI Express clocks are generated from a low bandwidth, high phase noise PLL frequency synthesizer. In these systems, a jitter attenuator may be required to attenuate high frequency random and deterministic jitter components from the PLL synthesizer and from the system board. The chip can be bypassed by inserting shunts into “P5” and “P6” jumper headers.

Figure (6) and Table (4) illustrate the implementation of the attenuator chip and output frequency selection modes.

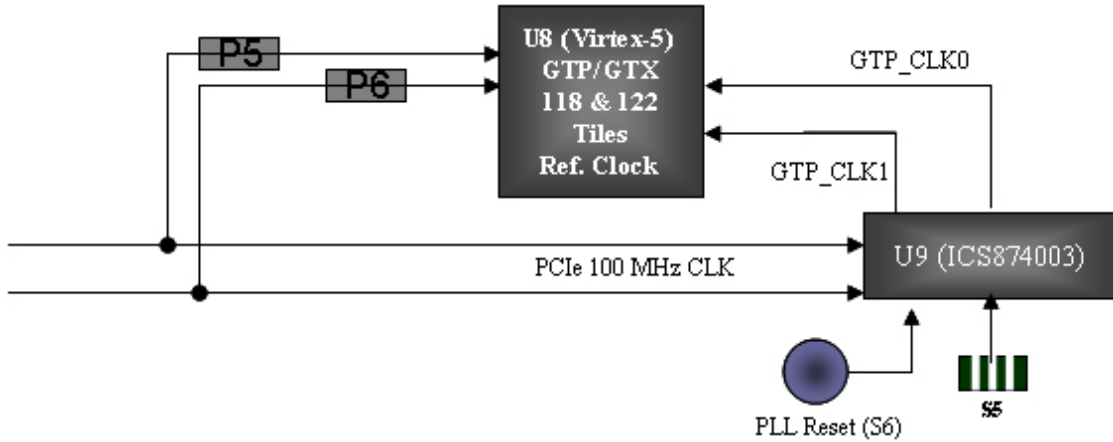


Figure (6) PCI Express Jitter Attenuator Diagram

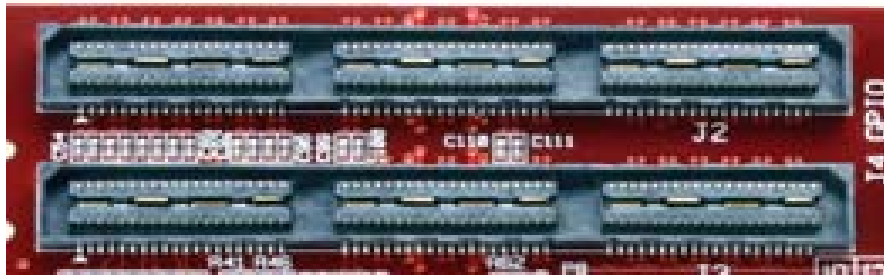
INPUT (S5)			OUTPUT
F_SEL2	F_SEL1	F_SEL0	QA0/nQA0, QA1/nQA1
0	0	0	DIV2 (250 MHz when input = 100 MHz)
1	0	0	DIV5 (100 MHz when input = 100 MHz)
0	1	0	DIV4 (125 MHz when input = 100 MHz)
1	1	0	DIV2 (250 MHz when input = 100 MHz)
0	0	1	DIV2 (250 MHz when input = 100 MHz)
1	0	1	DIV5 (100 MHz when input = 100 MHz)
0	1	1	DIV4 (125 MHz when input = 100 MHz)
1	1	1	DIV4 (125 MHz when input = 100 MHz)

Table (4) PCI Express Jitter Attenuator Mode Select

Notes:

- The default setting of “S5” is “101” for the LXT/SXT based boards (PCIe Gen1). With this setting a lower- jitter 100 MHz clock is applied across the GTP 118 and 122 GTP reference clock (recommended)
- The default setting of “S5” is “000” for the FXT based boards (PCIe Gen 2). With this setting a lower- jitter 250 MHz clock is applied across the GTX 118 and 122 GTX reference clock (recommended)

2.9.1) High-Speed LVDS or Single-Ended I/Os



The V5-PCIE2 board provides access to **50** pairs of LVDS IOs (2.5V) or 100 Single-Ended (3.3V) through two high-speed Samtec connectors (J2 and J3). The IO banks' (3, 12, 19, and 20) voltages are controlled via JP7 and JP8 as illustrated by the figure (7).

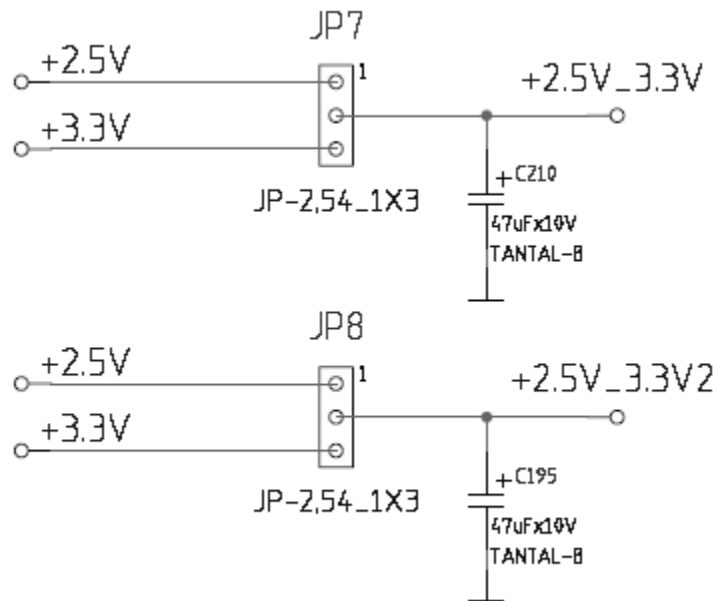


Figure (7): IO Bank Voltage Selection (2.5V or 3.3V)

The entire J2 connector (upper) is populated with LVDS/Single-Ended IOs (34 pairs/68 single). Half of the J3 connector (lower) is populated with LVDS/Single-Ended IOs (16pairs/32 single). Other half of the J3 connector is populated with 8 data-rate-adjustable RocketIO ports (section 2.5.2)

In addition to many GND pins, each connector provides 2.5V and 3.3V power supplies for add-on modules. A pair of differential clock is also available on each connector.

- High-Speed Connector's Part #: QSE-060-01-F-D-A <http://www.samtec.com/fppub/cpdf/QSE-XXX-01-X-D-XXX-MKT.pdf>

In addition to the QTE mating connectors (used on add-on daughter cards interfacing the V5-PCIE2 boards), Samtec also offers wide variety of mating cables and connectors. The following 6-inche QSE to QSE cable is available through HiTech Global : (Part Number: QSE-TO-QSE)



The high speed connectors can be used for connecting add-on modules to the V5-PCIE2 board. The “J32” with 3.3V and “J33” with 5.0V provide power supply and higher current to any customized add-on module (these jumpers can also be used for powering up cooling fans).

2.9.2) Data-Rate-Adjustable RocketIO GTP/GTX Serial Transceivers

The V5-PCIE2 provides access to 8 data-rate-adjustable RocketIO GTP/GTX ports. These ports are available on the “J3” high-speed connector as illustrated in table (9). The reference clock for the GTP/GTX tiles (GTP/GTX 112, 114, 116, and 120) is provided by the on-board Super Clock. The Super Clock can provide different output frequencies based on crystal values selected for the “U1”, “ZQ1”, and “ZQ2”. As illustrated in table (5), (6), and (7), the “S1” and “S4” Dip Switches control different division and selection modes.

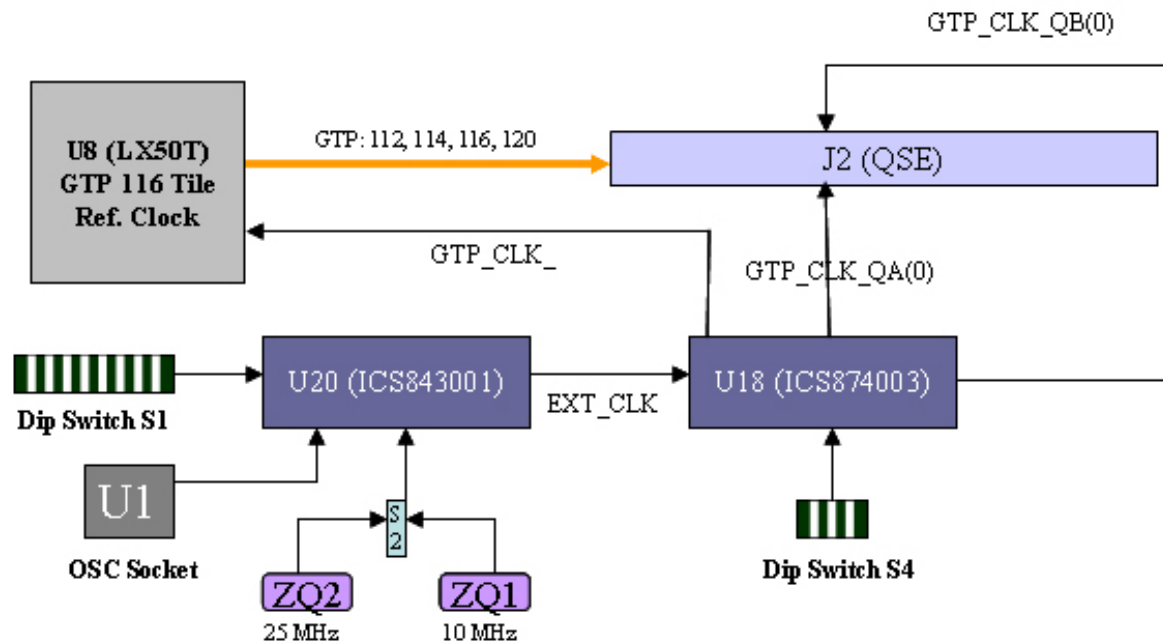


Figure (8): Super Clock Diagram

- Note (1):** The “GTP_CLK_” and “GTP_CLK_QA(0)” always have the same value
- Note (2):** Depending on setting of the “S4”, the “GTP_CLK_QA(0)” and “GTP_QB(0)” can have the same or different values

Inputs			M Divider Value	Input Frequency (MHz)	
M2 (S1: 8 th key)	M1 (S1: 7 th key)	M0 (S1: 6 th key)		Minimum	Maximum
0	0	0	18	31.1	38.9
0	0	1	22	25.5	31.8
0	1	0	24	23.3	29.2
0	1	1	25	22.4	28.0
1	0	0	32	17.5	21.9
1	0	1	40	14.0	17.5

Table (5) ICS843001-2 (U20) Programmable “M” Output Divider Function Table

Inputs			M Divider Value
N2 (S1: 3 rd key)	N1 (S1: 2 nd key)	N0 (S1: 1 st key)	
0	0	0	1
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	5
1	0	1	6
1	1	0	8
1	1	1	10

Table (6) ICS843001-2 (U20) Programmable “N” Output Divider Function Table

ICS843001 user manual is available at : <http://www.idt.com/products/getDoc.cfm?docID=15132337>

Inputs (S4)			Outputs	
F_SEL2 (S4: 1 st key)	F_SEL1 (S4: 2 nd key)	F_SEL0 (S4: 3 rd key)	QA0/nQA0, QA0/nQA0	QB0/nQB0
0	0	0	2÷	2÷
1	0	0	5÷	2÷
0	1	0	4÷	2÷
1	1	0	2÷	4÷
0	0	1	2÷	5÷
1	0	1	5÷	4÷
0	1	1	4÷	5÷
1	1	1	4÷	4÷

Table (7) ICS874003-2 (U18) F_SEL[2:0] Function Table

ICS874003-2 user manual is available at: <http://timing.idt.com/datasheets/ics874003.pdf>

Table (8) and (9) illustrate pin assignment for each high-speed QSE connector.

Upper Connector (J2)					
Pin #	Signal Name	FPGA Pin & Bank #	Pin #	Signal Name	FPGA Pin & Bank #
1	LVDS0_P	P7 (12)	2	LVDS1_P	R6 (12)
3	LVDS0_N	P6 (12)	4	LVDS1_N	T6 (12)
5	GND		6	GND	
7	LVDS2_P	M6 (12)	8	LVDS3_P	N8 (12)
9	LVDS2_N	M5 (12)	10	LVDS3_N	N7 (12)
11	GND		12	GND	
13	LVDS4_P	M7 (12)	14	LVDS5_P	K7 (12)
15	LVDS4_N	L6 (12)	16	LVDS5_N	K6 (12)
17	GND		18	GND	
19	LVDS6_P	G6 (12)	20	LVDS7_P	H7 (12)
21	LVDS6_N	G7 (12)	22	LVDS7_N	J7 (12)
23	GND		24	GND	
25	LVDS8_P	F9 (20)	26	LVDS9_P	G8 (20)
27	LVDS8_N	F8 (20)	28	LVDS9_N	H8 (20)
29	GND		30	GND	
31	LVDS10_P	F10 (20)	32	LVDS11_P	H10 (20)
33	LVDS10_N	G10 (20)	34	LVDS11_N	H9 (20)
35	GND		36	GND	
37	LVDS12_P	F11 (20)	38	LVDS13_P	G11 (20)
39	LVDS12_N	E11 (20)	40	LVDS13_N	G12 (20)
41	LVDS14_P	D11 (20)	42	LVDS15_P	E12 (20)
43	LVDS14_N	D10 (20)	44	LVDS15_N	E13 (20)
45	GND		46	GND	
47	LVDS_R(0)_P	F13 (20)	48	LVDS_R(1)_P	D12 (20)
49	LVDS_R(0)_N	G13 (20)	50	LVDS_R(1)_N	C12 (20)
51	GND		52	GND	
53	2.5V		54	3.3V	
55	2.5V		56	3.3V	
57	GND		58	GND	
59	DIFFCLK 0_P	H17 (3)	60	DIFFCLK1_P	J14 (3)
61	DIFFCLK 0_N	H18 (3)	62	DIFFCLK1_N	H13 (3)
63	GND		64	GND	
65	2.5V		66	3.3V	
67	2.5V		68	3.3V	
69	GND		70	GND	
71	LVDS16_P	K11 (20)	72	LVDS17_P	K8 (20)
73	LVDS16_N	J11 (20)	74	LVDS17_N	K9 (20)
75	GND		76	GND	
77	LVDS18_P	M10 (20)	78	LVDS19_P	M8 (20)
79	LVDS18_N	L9 (20)	80	LVDS19_N	L8 (20)

81	GND		82	GND	
83	GND		84	GND	
85	LVDS20_P	K17 (3)	86	LVDS21_P	L19 (3)
87	LVDS20_N	L18 (3)	88	LVDS21_N	K19 (3)
89	GND		90	GND	
91	LVDS22_P	R24 (19)	92	LVDS23_P	J20 (3)
93	LVDS22_N	T24 (19)	94	LVDS23_N	J21 (3)
95	GND		96	GND	
97	LVDS24_P	K24 (19)	98	LVDS25_P	L25 (19)
99	LVDS24_N	L24 (19)	100	LVDS25_N	L26 (19)
101	GND		102	GND	
103	LVDS26_P	J27 (19)	104	LVDS27_P	J24 (19)
105	LVDS26_N	J26 (19)	106	LVDS27_N	J25 (19)
107	GND		108	GND	
109	LVDS28_P	F25 (19)	110	LVDS29_P	G25 (19)
111	LVDS28_N	F26 (19)	112	LVDS29_N	G26 (19)
113	GND		114	GND	
115	LVDS30_P	E26 (19)	116	LVDS31_P	E28 (19)
117	LVDS30_N	E27 (19)	118	LVDS31_N	F28 (19)
119	GND		120	GND	

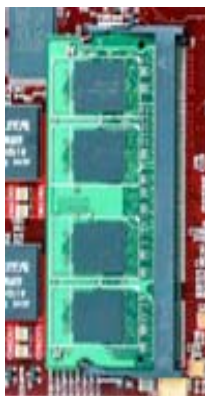
Table (8) High-Speed LVDS Connectors Summary – Upper Connector (J3)

Lower Connector (J3)					
Pin #	Signal Name	FPGA Pin & Bank #	Pin #	Signal Name	FPGA Pin & Bank #
1	GTP/GTX_RX_P(0)	AB1 (GTP 114)	2	GTP/GTX_TX_P(0)	AC2 (GTP 114)
3	GTP/GTX_RX_N(0)	AA1 (GTP 114)	4	GTP/GTX_TX_N(0)	AB2 (GTP 114)
5	GND		6	GND	
7	GTP/GTX_RX_P(1)	W1 (GTP 114)	8	GTP/GTX_TX_P(1)	V2 (GTP 114)
9	GTP/GTX_RX_N(1)	Y1 (GTP 114)	10	GTP/GTX_TX_N(1)	W2 (GTP 114)
11	GND		12	GND	
13	GTP/GTX_RX_P(2)	T1 (GTP 112)	14	GTP/GTX_TX_P(2)	U2 (GTP 112)
15	GTP/GTX_RX_N(2)	R1 (GTP 112)	16	GTP/GTX_TX_N(2)	T2 (GTP 112)
17	GND		18	GND	
19	GTP/GTX_RX_P(3)	N1 (GTP 112)	20	GTP/GTX_TX_P(3)	M2 (GTP 112)
21	GTP/GTX_RX_N(3)	P1 (GTP 112)	22	GTP/GTX_TX_N(3)	N2 (GTP 112)
23	GND		24	GND	
25	GTP_CLK_BUFF_QA(0)_P	U18 Pin# 3	26	GTP_CLK_BUFF_QB(0)_P	U18 Pin# 18
27	GTP_CLK_BUFF_QA(0)_N	U18 Pin# 4	28	GTP_CLK_BUFF_QB(0)_N	U18 Pin# 17
29	GND		30	GND	
31	GTP/GTX_RX_P(4)	K1 (GTP 116)	32	GTP/GTX_TX_P(4)	L2 (GTP 116)
33	GTP/GTX_RX_N(4)	J1 (GTP 116)	34	GTP/GTX_TX_N(4)	K2 (GTP 116)
35	GND		36	GND	
37	GTP/GTX_RX_P(5)	G1 (GTP 116)	38	GTP/GTX_TX_P(5)	F2 (GTP 116)

39	GTP/GTX_RX_N(5)	H1 (GTP 116)	40	GTP/GTX_TX_N(5)	G2 (GTP 116)
41	GTP/GTX_RX_P(6)	D1 (GTP 120)	42	GTP/GTX_TX_P(6)	E2 (GTP 120)
43	GTP/GTX_RX_N(6)	C1 (GTP 120)	44	GTP/GTX_TX_N(6)	D2 (GTP 120)
45	GND		46	GND	
47	LVDS_R(2)_P	B13 (20)	48	LVDS_R(3)_P	A13 (20)
49	LVDS_R(2)_N	C13 (20)	50	LVDS_R(3)_N	B12 (20)
51	GND		52	GND	
53	2.5V		54	3.3V	
55	2.5V		56	3.3V	
57	GND		58	GND	
59	DIFFCLK 2_P	H14 (3)	60	DIFFCLK3_P	J16 (3)
61	DIFFCLK 2_N	H15 (3)	62	DIFFCLK3_N	J17 (3)
63	GND		64	GND	
65	2.5V		66	3.3V	
67	2.5V		68	3.3V	
69	GND		70	GND	
71	GTP/GTX_RX_P(7)	A3 (GTP 120)	72	GTP/GTX_TX_P(7)	B4 (GTP 120)
73	GTP/GTX_RX_N(7)	A2 (GTP 120)	74	GTP/GTX_TX_N(7)	B3 (GTP 120)
75	GND		76	GND	
77	LVDS32_P	R7 (12)	78	LVDS33_P	N10 (20)
79	LVDS32_N	R8 (12)	80	LVDS33_N	N9 (20)
81	GND		82	GND	
83	GND		84	GND	
85	LVDS34_P	H19 (3)	86	LVDS35_P	K18 (3)
87	LVDS34_N	H20 (3)	88	LVDS35_N	J19 (3)
89	GND		90	GND	
91	LVDS36_P	P25 (19)	92	LVDS37_P	P26 (19)
93	LVDS36_N	N25 (19)	94	LVDS37_N	P27 (19)
95	GND		96	GND	
97	LVDS38_P	G27 (19)	98	LVDS39_P	H25(19)
99	LVDS38_N	H27 (19)	100	LVDS39_N	H24 (19)
101	GND		102	GND	
103	LVDS40_P	K28 (19)	104	LVDS41_P	K27 (19)
105	LVDS40_N	L28 (19)	106	LVDS41_N	K26 (19)
107	GND		108	GND	
109	LVDS42_P	M25 (19)	110	LVDS43_P	H28 (19)
111	LVDS42_N	M26 (19)	112	LVDS43_N	G28 (19)
113	GND		114	GND	
115	LVDS44_P	N24 (19)	116	LVDS45_P	M28 (19)
117	LVDS44_N	P24 (19)	118	LVDS45_N	N28 (19)
119	GND		120	GND	

Table (9) High-Speed LVDS & Rocket IO GTP Connectors Summary – Lower Connector (J2)

2.10) DDR 2 SODIM



The V5-PCIE2 board is populated with a 200-pin SO-DIMM connector which supports installation of Dual-Rank DDR2 SDRAM SO-DIMMs up to 4 GB (DDR2-533 and/or DDR2-400). The board is delivered with 512 MB Elpida DDR-2 SO-DIMM. Additional information is available at: <http://www.elpida.com/pdfs/E1084E20.pdf>

DDR-2 Memory Controller IP Core is available through HiTech Global. Additional information is available at <http://www.hitechglobal.com/IPCores/DDR2Controller.htm>. The V5-PCIE2 is also Xilinx MIG compatible.

Connector Pin Numbers/Pin Names, Signal Names, FPGA Pin Numbers, and banks are summarized in Table (10) and (11)

SO-DIMM Front Side				
Connector Pin #	Connector Pin Name	Signal Name	FPGA Pin #	Bank #
1	VREF 1	VCC0V9_VREF		
3	VSS 1	GND		
5	DQ0	DIMM_DQ0	AH29	17
7	DQ1	DIMM_DQ1	AJ30	17
9	VSS 2	GND		
11	DQS0#	DIMM_DQS0_N	AN32	13
13	DQS0	DIMM_DQS0_P	AP32	13
15	VSS 3	GND		
17	DQ2	DIMM_DQ2	AJ31	17
19	DQ3	DIMM_DQ3	AK31	17
21	VSS 4	GND		
23	DQ8	DIMM_DQ8	AH30	17
25	DQ9	DIMM_DQ9	AG30	17
27	VSS 5	GND		
29	DQS1#	DIMM_DQS1_N	AC30	13
31	DQS1	DIMM_DQS1_P	AB30	13
33	VSS 6	GND		
35	DQ10	DIMM_DQ10	AF29	17
37	DQ11	DIMM_DQ11	W27	17

39	VSS_7	GND		
41	VSS_8	GND		
43	DQ16	DIMM_DQ16	AA30	17
45	DQ17	DIMM_DQ17	AA29	17
47	VSS_9	GND		
49	DQS2#	DIMM_DQS2_N	Y29	13
51	DQS2	DIMM_DQS2_P	Y28	13
53	VSS_10	GND		
55	DQ18	DIMM_DQ18	W26	17
57	DQ19	DIMM_DQ19	W24	17
59	VSS_11	GND		
61	DQ24	DIMM_DQ24	U31	11
63	DQ25	DIMM_DQ25	U32	11
65	VSS_12	GND		
67	DM3	DIMM_DM3	U33	11
69	NC_1	4.7K Resistor		
71	VSS_13	GND		
73	DQ26	DIMM_DQ26	T33	11
75	DQ27	DIMM_DQ27	T34	11
77	VSS_14	GND		
79	CKE0	DIMM_CKE	AM33	13
81	VDD_1	VCC1V8		
83	NC_2	4.7K Resistor		
85	NC/BA2	DIMM_BA2	AN33	13
87	VDD_2	VCC1V8		
89	A12	DIMM_A12	AN34	13
91	A9	DIMM_A9	AL34	13
93	A8	DIMM_A8	AK34	13
95	VDD_3	VCC1V8		
97	A5	DIMM_A5	AH34	13
99	A3	DIMM_A3	AS34	13
101	A1	DIMM_A1	AE33	13
103	VDD_4	VCC1V8		
105	A10/AP	DIMM_A10	AD34	13
107	BA0	DIMM_BA0	AC34	13
109	WE#	DIMM_WE_N	AA34	13
111	VDD_5	VCC1V8		
113	CAS#	DIMM_CAS_N	Y34	13
115	S1#	DIMM_CS_N	Y33	13
117	VDD_6	VCC1V8		
119	ODT1	DIMM_ODT	V33	13
121	VSS_15	GND		
123	DQ32	DIMM_DQ32	K33	11
125	DQ33	DIMM_DQ33	N32	11

127	VSS 16	GND		
129	DQS4#	DIMM_DQS4_N	J34	11
131	DQS4	DIMM_DQS4_P	H34	11
133	VSS 17	GND		
135	DQ34	DIMM_DQ34	F33	11
137	DQ35	DIMM_DQ35	E33	11
139	VSS 18	GND		
141	DQ40	DIMM_DQ40	E34	11
143	DQ41	DIMM_DQ41	C33	11
145	VSS 19	GND		
147	DM5	DIMM_DM5	B33	11
149	VSS 20	GND		
151	DQ42	DIMM_DQ42	A33	11
153	DQ43	DIMM_DQ43	B32	11
155	VSS 21	GND		
157	DQ48	DIMM_DQ48	R31	15
159	DQ49	DIMM_DQ49	P31	15
161	VSS 22	GND		
163	NC 3	4.7K Resistor		
165	VSS 23	GND		
167	DQS6#	DIMM_DQS6_N	P29	15
169	DQS6	DIMM_DQS6_P	N29	15
171	VSS 24	GND		
173	DQ50	DIMM_DQ50	T31	15
175	DQ51	DIMM_DQ51	M30	15
177	VSS 25	GND		
179	DQ56	DIMM_DQ56	L30	15
181	DQ57	DIMM_DQ57	R27	15
183	VSS 26	GND		
185	DM7	DIMM_DM7	H30	15
187	VSS 27	GND		
189	DQ58	DIMM_DQ58	J31	15
191	DQ59	DIMM_DQ59	F29	15
193	VSS 28	GND		
195	SDA	DIMM_SDA	E31	15
197	SCL	DIMM_SCL	E29	15
199	VDDSPD	VCC1V8		

Table (10) DDR2 Memory Connections Summary (Front Side)

SO-DIMM Back Side				
Connector Pin #	Connector Name	Signal Name	FPGA Pin #	Bank #
2	VSS 29	GND		
4	DQ4	DIMM_DQ4	AF30	17
6	DQ5	DIMM_DQ5	AF31	17
8	VSS 30	GND		
10	DM0	DIMM_DM0	AE29	17
12	VSS 31	GND		
14	DQ6	DIMM_DQ6	AD30	17
16	DQ7	DIMM_DQ7	AD29	17
18	VSS 32	GND		
20	DQ12	DIMM_DQ12	AC29	17
22	DQ13	DIMM_DQ13	V24	17
24	VSS 33	GND		
26	DM1	DIMM_DM1	Y31	17
28	VSS 34	GND		
30	CK0	DIMM_CLK0_P	V28	17
32	CK0#	DIMM_CLK0_N	V27	17
34	VSS 35	GND		
36	DQ14	DIMM_DQ14	V30	17
38	DQ15	DIMM_DQ15	V29	17
40	VSS 36	GND		
42	VSS 37	GND		
44	DQ20	DIMM_DQ20	W31	17
46	DQ21	DIMM_DQ21	W29	17
48	VSS 38	GND		
50	NC4	4.7 K Resistor		
52	DM2	DIMM_DM2	Y27	17
54	VSS 39	GND		
56	DQ22	DIMM_DQ22	W25	17
58	DQ23	DIMM_DQ23	V25	17
60	VSS 40	GND		
62	DQ28	DIMM_DQ28	R32	11
64	DQ29	DIMM_DQ29	R33	11
66	VSS 41	GND		
68	DQS3#	DIMM_DQS3_N	K34	11
70	DQS3	DIMM_DQS3_P	L34	11
72	VSS 42	GND		
74	DQ30	DIMM_DQ30	R34	11
76	DQ31	DIMM_DQ31	P34	11
78	VSS 43	GND		
80	CLKE1	DIMM_CKE	AM32	13

82	VDD 7	VCC1V8		
84	NC5	DIMM_A15	AP32	13
86	NC6	DIMM_A14	AN32	13
88	VDD 8	VCC1V8		
90	A11	DIMM_A11	AL33	13
92	A7	DIMM_A7	AK33	13
94	A6	DIMM_A6	K32	13
96	VDD 9	VCC1V8		
98	A4	DIMM_A4	AJ34	13
100	A2	DIMM_A2	AF33	13
102	A0	DIMM_A0	Y33	13
104	VDD 10	VCC1V8		
106	BA1	DIMM_BA1	AD32	13
108	RAS#	DIMM_RAS_N	AB33	13
110	S0#	DIMM_S0_N	AA33	13
112	VDD 11	VCC1V8		
114	ODT0	DIMM_ODT	W34	13
116	A13	DIMM_A13	V34	13
118	VDD 12	VCC1V8		
120	NC7	4.7K Resistor		
122	VSS 44	GND		
124	DQ36	DIMM_DQ36	P32	11
126	DQ37	DIMM_DQ37	M32	11
128	VSS 45	GND		
130	DM4	DIMM_DM4	L33	11
132	VSS 46	GND		
134	DQ38	DIMM_DQ38	G33	11
136	DQ39	DIMM_DQ39	LF34	11
138	VSS 47	GND		
140	DQ44	DIMM_DQ44	D34	11
142	DQ45	DIMM_DQ45	K32	11
144	VSS 48	GND		
146	DQS5#	DIMM_DQS5_N	H33	11
148	DQS5	DIMM_DQS5_P	J32	11
150	VSS 49	GND		
152	DQ46	DIMM_DQ46	E32	11
154	DQ47	DIMM_DQ47	G32	11
156	VSS 50	GND		
158	DQ52	DIMM_DQ52	T26	15
160	DQ53	DIMM_DQ53	T28	15
162	VSS 51	GND		
164	CK1	DIMM_CLK1_P	C32	11
166	CK1#	DIMM_CLK1_N	D32	11
168	VSS 52	GND		

170	DM6	DIMM_DM6	U28	15
172	VSS_53	GND		
174	DQ54	DIMM_DQ54	U30	15
176	DQ55	DIMM_DQ55	P30	15
178	VSS_54	GND		
180	DQ60	DIMM_DQ60	J30	15
182	DQ61	DIMM_DQ61	J29	15
184	VSS_55	GND		
186	DQS7#	DIMM_DQS7_N	L31	15
188	DQS7	DIMM_DQS7_P	K31	15
190	VSS_56	GND		
192	DQ62	DIMM_DQ62	H29	15
194	DQ63	DIMM_DQ63	F30	15
196	VSS_57	GND		
198	SA0	DIMM_SA0	F31	15
200	SA1	DIMM_SA1	G31	15

Table (11) DDR2 Memory Connections Summary (Back Side)

2.11) DDR-3

The V5-PCIE2 board is populated with 512 MB Elpida DDR-3 component (EDJ1116BASE-AE-E FBGA-96).

Features

- Double-data-rate architecture; two data transfers per clock cycle
- The high-speed data transfer is realized by the 8 bits prefetch pipelined architecture
- Bi-directional differential data strobe (DQS and /DQS) is transmitted/received with data for capturing data at the receiver
- DQS is edge-aligned with data for READs; center aligned with data for WRITEs
- Differential clock inputs (CK and /CK)
- DLL aligns DQ and DQS transitions with CK transitions
- Commands entered on each positive CK edge; data and data mask referenced to both edges of DQS
- Data mask (DM) for write data
- Posted /CAS by programmable additive latency for better command and data bus efficiency
- On-Die Termination (ODT) for better signal quality
 - Synchronous ODT
 - Dynamic ODT
 - Asynchronous ODT
- Multi Purpose Register (MPR) for temperature read out
- ZQ calibration for DQ drive and ODT
- Programmable Partial Array Self-Refresh (PASR)
- /RESET pin for Power-up sequence and reset function
- SRT range:
 - Normal/extended
 - Auto/manual self-refresh
- Programmable Output driver impedance control

Additional product information is available at <http://www.elpida.com/pdfs/E1128E20.pdf>

DDR-3 Memory Controller IP Core is available through HiTech Global. Additional information is available at <http://www.hitechglobal.com/IPCores/DDR3Controller.htm>

DDR 3 Component Pin #	Signal Name	FPGA Pin #	Bank #
N3	DDR3_A[0]	W6	18
P7	DDR3_A[1]	AE6	18
P3	DDR3_A[2]	AD6	18
N2	DDR3_A[3]	Y7	18
P8	DDR3_A[4]	AD6	18
P2	DDR3_A[5]	AD5	18
R8	DDR3_A[6]	AD4	18
R2	DDR3_A[7]	Y8	18
T8	DDR3_A[8]	AD7	18
R3	DDR3_A[9]	AC7	18
L7	DDR3_A[10]	AB6	18
R7	DDR3_A[11]	AC5	18
N7	DDR3_A[12]	AB7	18
D7	DDR3_DQ_BY0_B[0]	AL11	22
C3	DDR3_DQ_BY0_B[1]	AM11	22
C8	DDR3_DQ_BY0_B[2]	AM12	22
C2	DDR3_DQ_BY0_B[3]	AP12	22
A7	DDR3_DQ_BY0_B[4]	AM13	22
A2	DDR3_DQ_BY0_B[5]	AN13	22
B8	DDR3_DQ_BY0_B[6]	AP14	22
A3	DDR3_DQ_BY0_B[7]	AN14	22
E3	DDR3_DQ_BY1_B[0]	AG11	22
F7	DDR3_DQ_BY1_B[1]	AG10	22
F2	DDR3_DQ_BY1_B[2]	AH8	22
F8	DDR3_DQ_BY1_B[3]	AG8	22
H3	DDR3_DQ_BY1_B[4]	AH10	22
H8	DDR3_DQ_BY1_B[5]	AH9	22
G2	DDR3_DQ_BY1_B[6]	AE11	22
H7	DDR3_DQ_BY1_B[7]	AF11	22
C7	DDR3_DQS_BY0_P	AD10	22
B7	DDR3_DQS_BY0_N	AD11	22
F3	DDR3_DQS_BY1_P	AK11	22
G3	DDR3_DQS_BY1_N	AJ11	22
L2	DDR3_CS_N	V8	18
J3	DDR3_RAS_N	AK6	18
K3	DDR3_CAS_N	AK7	18
L3	DDR3_WE_N	U8	18
K9	DDR3_CKE	V9	18
K1	DDR3_ODT	W10	18
M3	DDR3_BA[2]	Y6	18
N8	DDR3_BA[1]	AE7	18
M2	DDR3_BA[0]	AF6	18
T2	DDR3_RST_N	W7	18
D3	DDR3_DM_BY0	AK9	22

E7	DDR3_DM_BY1	AF9	22
J7	DDR3_CK_P	AE8	22
K7	DDR3_CK_N	AD9	22
H1	VREFCA	AN12	22
M8	VREFDQ	AF10	22
N1	VDD1	AF7	22
R1	VDD2	AH11	22
B2	VDD3	AJ8	22
K2	VDD4	DDR3-VCC	N/A
G7	VDD5	DDR3-VCC	N/A
K8	VDD6	DDR3-VCC	N/A
D9	VDD7	DDR3-VCC	N/A
N9	VDD8	DDR3-VCC	N/A
R9	VDD9	DDR3-VCC	N/A
A1	VDDQ1	DDR3-VCC	N/A
C1	VDDQ2	DDR3-VCC	N/A
F1	VDDQ3	DDR3-VCC	N/A
D2	VDDQ4	DDR3-VCC	N/A
A8	VDDQ5	DDR3-VCC	N/A
C9	VDDQ6	DDR3-VCC	N/A
E9	VDDQ7	DDR3-VCC	N/A
H2	VDDQ8	DDR3-VCC	N/A
H9	VDDQ9	DDR3-VCC	N/A
E1	VSS1	GND	N/A
M1	VSS2	GND	N/A
P1	VSS3	GND	N/A
T1	VSS4	GND	N/A
J2	VSS5	GND	N/A
B3	VSS6	GND	N/A
G8	VSS7	GND	N/A
J8	VSS8	GND	N/A
A9	VSS9	GND	N/A
M9	VSS10	GND	N/A
P9	VSS11	GND	N/A
T9	VSS12	GND	N/A
B1	VSSQ1	GND	N/A
D1	VSSQ2	GND	N/A
G1	VSSQ3	GND	N/A
E2	VSSQ4	GND	N/A
D8	VSSQ6	GND	N/A
E8	VSSQ7	GND	N/A
B9	VSSQ8	GND	N/A
F9	VSSQ9	GND	N/A
G9	VSSQ10	GND	N/A

Table (12) DDR3 Memory Connections Summary

2.12) 10/100/1000 Tri-Speed Ethernet PHY

The V5-PCIE2 board is populated with one Marvell Alaska PHY devices (88E1111) operating at 10/100/1000 Mb/s.

The Marvell Alaska PHY device enables copper 1000BASE-T Gigabit Interface Converter (GBIC) modules as well as Small Form Factor Pluggable (SFP) modules. The single-port Alaska family offers additional support of 1000BASE-X through an integrated 1.25 GHz Serializer/Deserializer (SERDES), enabling the use of the device in fiber-optic Gigabit Ethernet applications (IEEE 802.3z). The Marvell Alaska devices include advanced features such as:

- Virtual Cable Tester™ (VCT) cable diagnostic
- Media Detect feature
- Low power consumption
- Small footprint
- 2/3-Pair Downshift

The V5-PCIE2 board supports MII, GMII, and RGM interface modes with the FPGA. The PHY is connected to one hard-coded 10/100/1000 Ethernet Media Access Controllers (MAC) inside the Virtex-5 FPGA. The other sides of the PHY is connected to one Halo HFJ11-1G01E RJ-45 Connector with built-in magnetic.

A 25-MHz crystal (ZQ3) supplies the clock signal to the PHY. The PHY is configured to default at power-on or reset (these settings may be overwritten via software). I/O connections to the Ethernet PHY are summarized in Table (13)

Pin	Bit[2]	Bit[1]	Bit[0]		
CONFIG0	PHYADR[2]	PHYADR[1]	PHYADR[0]	000	PHYAddress "00000". Do not advertise the PAUSE bit
CONFIG1	ENA_PAUSE	PHYADR[4]	PHYADR[3]	000	
CONFIG2	ANEG[3]	ANEG[2]	ANEG[1]	111	Auto-Neg enabled, advertise all capabilities; prefer slave. Auto crossover enabled. 125 CLK option disabled.
CONFIG3	ANEG[0]	ENA_XC	DIS_125	111	
CONFIG4	HWCFG_MODE[2]	HWCFG_MODE[1]	HWCFG_MODE[0]	XXX	GMII to Cu mode. Fiber/copper auto-detect disabled. Sleep mode disabled.
CONFIG5	DIS_FC	DIS_SLEEP	HWCFG_MODE[3]	111	
CONFIG6	SEL_BDT	INT_POL	75/50 OHM	010	MDC/MDIO selected. Active LOW Interrupt. 50 Ohm SERDES option.

Table (13) PHY Configuration

Pin to Constant Mapping	
Pin	Bit[2:0]
+2.5V	111
LED_LINK10	110
LED_LINK100	101
LED_LINK1000	100
LED_DUPLEX	011
LED_RX	010
LED_TX	001
GND	000

Table (14) Link Status Summary

10/100/1000 Ethernet Jumper Setting:

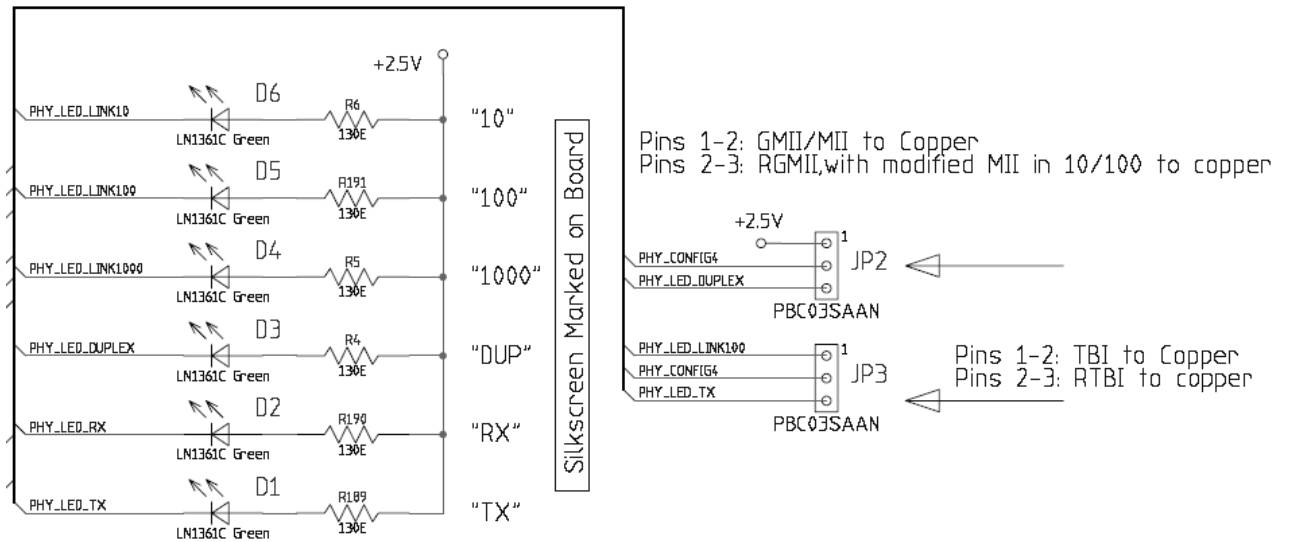


Figure (9) Ethernet PHY Mode Jumper Setting

Ethernet PHY Component Pin #	Signal Name	FPGA Pin #	Bank #
24	PHY_MDIO	AE26	21
25	PHY_MDC	AF26	21
23	PHY_INT	AE27	21
27	PHY_COMA	AG26	21
28	PHY_RESET	AF25	21
30	PHY_RSET	AG25	21
84	PHY_CRS	AA28	21
83	PHY_COL	Y2	21
2	PHY_RXCLK	AA25	21
3	PHY_RXER	AA24	21
94	PHY_RXCTL_RXDV	AA26	21
95	PHY_RXD[0]	AC24	21
92	PHY_RXD[1]	AC27	21

93	PHY_RXD[2]	AC25	21
91	PHY_RXD[3]	AC28	21
90	PHY_RXD[4]	AB27	21
89	PHY_RXD[5]	AB28	21
87	PHY_RXD[6]	AD25	21
86	PHY_RXD[7]	AD24	21
8	PHY_TXC_GTXCLK	AD26	21
4	PHY_TXCLK	AB25	21
7	PHY_TXER	AD27	21
9	PHY_TXCTL_TXEN	AB26	21
11	PHY_TXD[0]	AF24	21
12	PHY_TXD[1]	AE24	21
14	PHY_TXD[2]	AK29	21
16	PHY_TXD[3]	AJ29	21
17	PHY_TXD[4]	AE28	21
18	PHY_TXD[5]	AF28	21
19	PHY_TXD[6]	AG27	21
20	PHY_TXD[7]	AG28	21
44	TDI	NC	
46	TMS	NC	
47	TRST_B	NC	
50	TDO	NC	
49	TCK	2.5 V	
26	VDDDX1	2.5 V	
48	VDDX2	2.5 V	
5	VDDO1	2.5 V	
21	VDDO2	2.5 V	
88	VDDO3	2.5 V	
96	VDDO4	2.5 V	
29	PHY_MDIP[0]_P		
31	PHY_MDIP[0]_N		
33	PHY_MDIP[1]_P		
34	PHY_MDIP[1]_N		
39	PHY_MDIP[2]_P		
41	PHY_MDIP[2]_N		
42	PHY_MDIP[3]_P		
43	PHY_MDIP[3]_N		
37	HSDAC_P		
38	HSDAC_N		
79	SCLK_P		
80	SCLK_N		
82	SIN_P		
81	SIN_N		
77	SOUT_P		
75	SOUT_N		
56	SEL_OSC		

55	XTAL1	ZQ3 (25MHZ)	
54	XTAL2	ZQ3 (25 MHZ)	
76	PHY_LED_LINK10		
74	PHY_LED_LINK100		
73	PHY_LED_LINK1000		
70	PHY_LED_DUPLEX		
69	PHY_LED_RX		
68	PHY_LED_TX		
65	CONFIG0	GND	
64	CONFIG1	GND	
63	CONFIG2	2.5V	
61	CONFIG3	2.5V	
60	PHY_CONFIG4		
59	CONFIG5	2.5V	
58	PHY_LED_RX		
32	AVDD1	PHY_AVDD0	
35	AVDD2	PHY_AVDD0	
36	AVDD3	PHY_AVDD0	
40	AVDD4	PHY_AVDD0	
45	AVDD5	PHY_AVDD0	
78	AVDD6	PHY_AVDD0	
52	VDDOH1	2.5V	
66	VDDOH2	2.5V	
72	VDDOH3	2.5V	
1	DVDD1	1V FPGA CORE	
6	DVDD2	1V FPGA CORE	
10	DVDD3	1V FPGA CORE	
15	DVDD4	1V FPGA CORE	
57	DVDD5	1V FPGA CORE	
62	DVDD6	1V FPGA CORE	
67	DVDD7	1V FPGA CORE	
71	DVDD8	1V FPGA CORE	
85	DVDD9	1V FPGA CORE	

Table (15) Ethernet PHY Connections Summary

2.13) LEDs & Pushbuttons

2.13.1) User LEDs

The HTG-V5-PCIE2 provides eight user LEDs that can be turned ON by driving the LED signals to Ground.

Signal Name	Reference Designator	FPGA Pin #
V5_APP_LED (0)	D11	AH27
V5_APP_LED (1)	D12	AH28
V5_APP_LED (2)	D13	AK28
V5_APP_LED (3)	D14	AK26
V5_APP_LED (4)	D15	AJ27
V5_APP_LED (5)	D16	AK27
V5_APP_LED (6)	D17	AJ26
V5_APP_LED (7)	D18	AF19

Table (16) User LEDs

2.13.2) Configuration & INIT LEDs

The HTG-V5-PCIE2 provides INIT and DONE indicator LEDs, that are turned ON by the FPGA during the configuration process

Signal Name	Reference Designator	FPGA Pin #
XCF_wait	D8	N14
FPGA_Done	D9	M15

Table (17) Configuration & INIT LEDs

2.13.3) User Pushbuttons

The HTG-V5-PCIE2 provides three pushbutton switches. The S8 pushbutton initiates a full FPGA device configuration cycle while the board is powered on. The S7 pushbutton is for a user-assigned function. The S6 resets the PCIe Jitter Attenuator IC.

Signal Name	Reference Designator	Pin #
XCF_RP	S8	U8 (FPGA) – M22
V5_APP_SW	S7	U8 (FPGA) - AG18
RESET_PLL	S6	U9 (PCIe Jitter Attenuator) - 5

Table (18) User Pushbuttons

2.14) Configuration Options

The on-board FPGA can be configured directly via JTAG (J5) or the on-board 128 Mb Platform Flash XL (U11). The 128 Mb Flash can also be used for additional storage space.

2.14.1) Direct FPGA Configuration

- 1) Connect the 14-pin header of the Xilinx USB programming cable to the on-board “J5” connector. The USB header should be connected to USB port of a PC on the other side. The Xilinx ISE should already be installed on the PC.
- 2) Apply **5V** / 5+ Amp supply either to the “J6” (standard wall power supply) **OR** to the “J7” (ATX Power Connector). **Note: Applying higher supply voltages will damage the board.** The board can also be powered by 12V supply from standard motherboards (the SW1 should be in PCI position)



Figure (10) Configuration in Stand Alone Mode

- 3) Launch the ISE 10.1 “iMPACT” tool:
Start → **All Programs** → **Xilinx ISE** → **Accessories** → **iMPACT**.
- 4) Cancel the following window (iMPACT Project). This leads to verification of on-board Xilinx components.

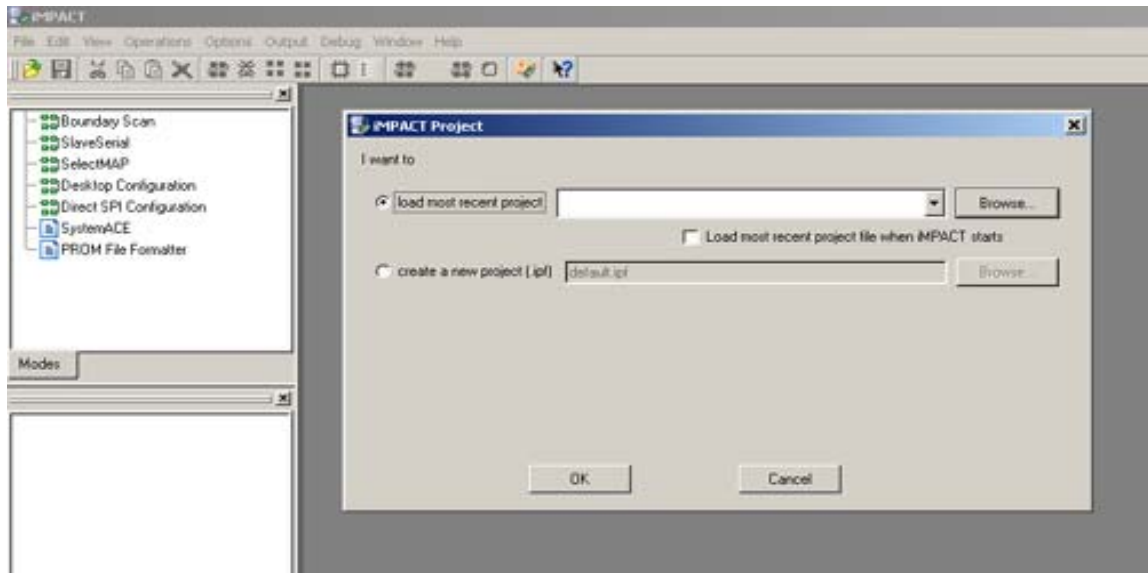


Figure (11)

- 5) Double Click on the “**Boundary Scan**” (the first item on the list) and Single Click on the “**Initialize Chain**” icon (the 7th icon from the left on the tool bar). This verifies correct connection between the board and PC by identifying the on-board Xilinx components.
- 6) Click on the FPGA image and select the desired configuration file (.bit)
- 7) After successful configuration the “DONE” LED illuminates.

2.14.2 Platform Flash Programming:

The V5-PCIE2 board is populated with the Xilinx 128 Mb Platform Flash XL which provides faster configuration speed and additional user storage space

The V5-PCIE2 board can be programmed in “BPI-UP”, “SSM”, “MSN” or “JTAG” mode. Using the “S3” Dip switch, users can select different configuration modes. Table (19) illustrates different mode selections:

Mode	M2	M1	M0
Byte-wide Peripheral Interface (BPI-UP)	0	1	0
Slave Serial Mode (SSM)	1	1	0
JTAG	1	0	1
Slave Serial Mode (MSM)	1	0	0

Table (19) Configuration Modes

The “JP9” jumper and “U10” (on-board 50 MHz clock) should be used for selecting the “**Slave**” or “**Master**” mode for the FPGA clocking.

JP9: ON = SSM

JP9: OFF = BPI UP or MSM

Note: the same 50 MHz clock can also be used as a user clock (via an on-board dual buffer with 3-state output and JP15)

Large memory size of the on-board Platform Flash XL can hold multiple bitstreams. Using the “S9” DIP switch, users can select up to 4 different configuration bitstreams without going through reprogramming the board.

Procedure (command mode)

```
Promgen -p mcs -x xcf128x -data_width 16 -o ./outputname.mcs -u 0 ./routedbit1.bit -u 200000  
./routedbit2.bit -u 400000 ./routedbit3.bit -u 600000 ./routedbit4.bit
```

To program the Flash in the command mode, create a cmd file either by using the log file from a GUI run or edit a file with the following.:

```
Programx128.cmd  
setMode -bs  
setCable -port auto  
identify  
attachflash -position 1 -bpi "XCF128X"  
assignfiletoattachedflash -position 1 -file "./outputname.mcs"  
attachflash -position 1 -bpi "XCF128X"  
Program -p 1 -bpionly -e -v  
quit
```

To start impact and program the FLASH in the command mode type:

```
impact -batch ./Programx128.cmd
```

Selecting Design to Configure

Switch S9 is the 2 upper address bits of the FLASH device A21 and A22. These select 1 of 4 possible designs to load from FLASH.

```
Design 1 (FLASH address 000000) S9 ON ON  
Design 2 (FLASH address 200000) S9 ON OFF  
Design 3 (FLASH address 400000) S9 OFF ON  
Design 4 (FLASH address 600000) S9 OFF OFF
```

Note: if the selected image is not present in the FLASH it will loop up and around to the next address.

The Xilinx Platform XL user manual provides detailed step-by-step procedure for indirect programming of the on-board 128 Mb platform flash. The most updated user manual is available at:

http://www.xilinx.com/support/documentation/user_guides/UG438.pdf

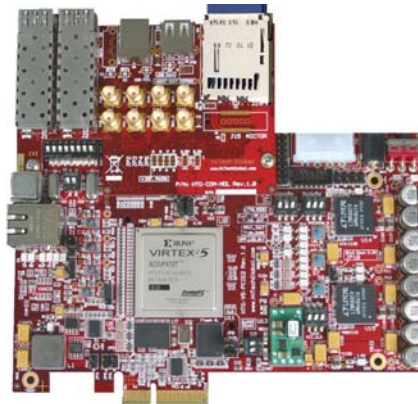
Chapter 3: Accessories

The V5-PCIE2 boards are supported by the following accessories:

3.1) Communication Module

Using the on-board high-speed connectors (J2 & J3), the communication module (HTG-COM-MDL) provides access to:

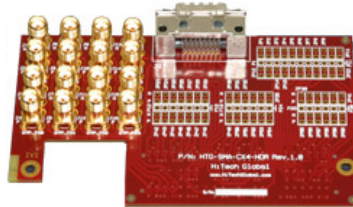
- x1 USB 2.0 (480 Mbps) & 3.0 (4.8 Gbps) Host – USB 3.0 support is available with the FXT based boards
- x1 USB (480 Mbps) & 3.0 (4.8 Gbps) Device
- x2 SFP
- x1 SATAII
- x8 SMA (2 RocketIO GTP/GTX ports)
- x1 SD interface
- x1 Debug port (Mictor)



3.2) CX4/SMA Module

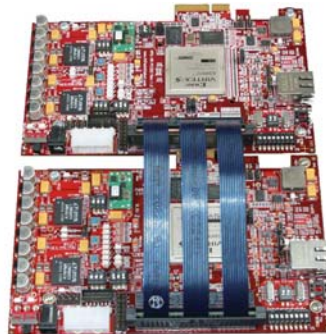
Using the on-board high-speed connectors (J2 & J3), the CX4/SMA module (HTG-SMA-CX4-HDR) provides access to:

- x1 CX4 (XAUI interface)
- x16 SMA (4 RocketIO GTP/GTX) Ports
- IO Headers



3.3) High-Speed Cable

Using the on-board high-speed connectors (J2 & J3), two V5-PCIE2 boards can be connected together via a Samtec high-speed cable (QSE-TO-QSE) to create a development environment with larger FPGA gate count and additional peripherals



3.4) Customized PC

Customized PCs with Linux and Windows operating systems are available to support flexible and user friendly PC environment for PCI Express Gen 1 & 2 developments. Additional product information is available at http://www.hitechglobal.com/Accessories/PCIExpress-Gen2_PC.htm



Chapter 4: PCI Express Software & Drivers

The V5-PCIE2 board is shipped with the evaluation version of PCIE drivers (WinDriver). The WinDriver evaluation is valid for period of 30 days. A complete list of PCI drivers are posted at: <http://hitechglobal.com/DesignTools/PCIDrivers.htm>

WinDriver is a development toolkit that dramatically simplifies the difficult task of creating device drivers and hardware access applications. WinDriver includes a wizard and code generation features that automatically detect your hardware and generate the driver to access it from your application. The driver and application you develop using WinDriver is source code compatible between all supported operating systems (WinDriver currently supports Windows 98/Me/NT/2000/XP/Server 2003/CE.NET, Linux, Solaris and VxWorks.). The driver is binary compatible between Windows 98/Me/NT/2000/XP/Server 2003. Bus architecture support includes PCI/PCMCIA/CardBus/ISA/EISA/CompactPCI/PCI Express (PCMCIA is supported only on Windows 2000/XP/Server 2003). WinDriver provides a complete solution for creating high-performance drivers.

Easy Development:

WinDriver enables Windows 98 / Me / NT / 2000 / XP / Server 2003 / CE.NET, Linux, Solaris and VxWorks programmers to create PCI/PCMCIA/CardBus/ISA/EISA/CompactPCI/PCI Express based device drivers in an extremely short time. WinDriver allows you to create your driver in the familiar user-mode environment, using MSDEV/Visual C/C++, MSDEV .NET, Borland C++ Builder, Borland Delphi, Visual Basic 6.0, MS eMbedded Visual C++, MS Platform Builder C++, GCC, or any other appropriate compiler. You do not need to have any device driver knowledge, nor do you have to be familiar with operating system internals, kernel programming, the DDK, ETK or DDI/DKI.

Cross Platform:

The driver created with WinDriver will run on Windows 98/Me/NT/2000/XP/Server 2003/CE.NET, Linux, Solaris and VxWorks. In other words - write it once, run it on many platforms.

Friendly Wizards:

DriverWizard (included) is a graphical diagnostics tool that lets you view/define the device's resources and test the communication with the hardware with just a few mouse clicks, before writing a single line of code. Once the device is operating to your satisfaction, DriverWizard creates the skeletal driver source code, giving access functions to all the resources on the hardware.

Kernel-Mode Performance:

WinDriver's API is optimized for performance.

For drivers that need kernel-mode performance, WinDriver offers the Kernel PlugIn. This powerful feature enables you to create and debug your code in user mode and run the performance-critical parts of your code (such as the interrupt handling or access to I/O mapped memory ranges) in kernel mode, thereby achieving kernel-mode performance (zero performance degradation). This unique feature allows the developer to run user-mode code in the OS kernel without having to learn how the kernel works.

There is no need to use the Kernel PlugIn when working with Windows CE or VxWorks, since there is no separation between user and kernel modes in these operating systems. This enables you to achieve optimal performance from user-mode code.

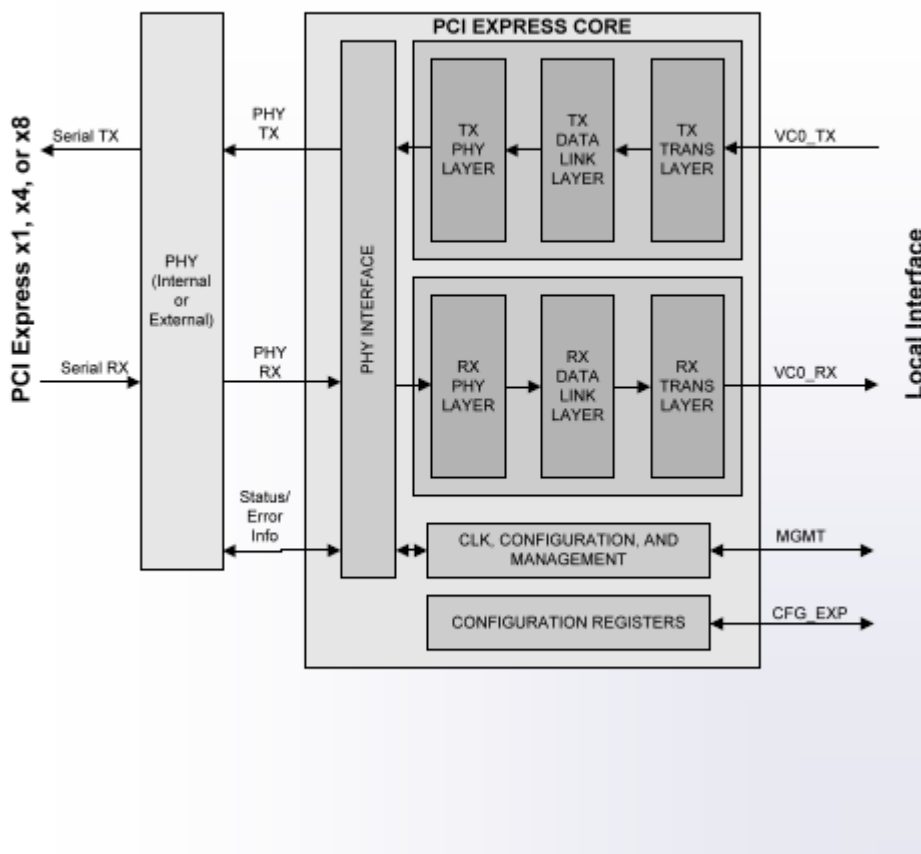
Chapter 5: Intellectual Property (IP) Cores

5.1) PCI Express

The V5-PCIE2 is designed to host any PCI Express PCI-SIG compliant Gen 1 and Gen 2 motherboard. The card can be used with the Integrated Endpoint Block for PCI Express which is compliant to the v1.1 base specification or can be used with a Soft IP core for PCI Express 1.1 or 2.0.

- High-performance, easy-to-use core
- Endpoint and Root Port support
- x1, x4, x8 lane versions available
- 32 and 64 bit address support
- Legacy interrupt and MSI support
- Status Port provides detailed access to low-level core status and data
- Complete PCI Express PHY support including integrated PHY FPGAs, discrete PHY chips and PIPE compliant ASIC PHYs
- Provided with a full-featured Verification Suite
- PCI Express Base Specification Revision 1.1 & 2.0 compliant
- Fully hardware validated and PCI-SIG certified

Block Diagram



5.1.1) PCI Express Back-End Features

Key features:

- PCI Express Core Support (Provides low-level PCI Express functionality)
 - o x1, and x4, PCI Express Core (soft core)
 - o x1, and x4, Xilinx PCI Express Endpoint Block Plus (Virtex 5 hard core)

- DMA Interface
 - o Very flexible, easy-to-use, high-performance DMA implementation
 - o Card-to-System (C2S) DMA Engine
 - _ Takes data from user logic and makes DMA Write Requests to system memory
 - _ Demand-driven user interface
 - _ Flexible Control - DMA Descriptor Engine fetches DMA Descriptors from a linked list of Descriptors stored in system memory or user logic can directly control the DMA Engine
 - o System-to-Card (S2C) DMA Engine
 - _ Makes DMA Read Requests from system memory, handles the resulting Read Completions, and forwards read data to user logic
 - _ Demand-driven user interface
 - _ Guarantees read data ordering (re-orders completions that were received out of order)
 - _ Flexible Control - DMA Descriptor Engine fetches DMA Descriptors from a linked list of Descriptors stored in system memory or user logic can directly control the DMA Engine
 - o Base Configuration has 1 Card to System DMA Engine and 1 System to Card DMA Engine
 - o Multi-Engine Configuration has 1-4 Card to System DMA Engines and 1-4 System to Card DMA Engines
 - o Engines are interleaved on a PCI Express packet basis
 - o 32-bit and 64-bit System Address Support
 - o 32-bit and 64-bit Descriptor Linked-List System Address Support
 - o Up to 64-bit Card Address Support
 - o Designed for DMA destination which are FIFOs or addressed memory
 - o MSI and Legacy Interrupt support
 - o System address, Card Address, and Byte Count support byte alignment allowing for maximum software flexibility
 - o Supports fragmented system and card memory
 - o Supports extremely long Descriptor chains

- Master Interface
 - o Simple interface supports generation of Memory (32/64-bit address), I/O, Configuration (Root Complex implementations only), and Message (Msg/MsgD) transactions
 - o Supports write and read transactions with up to one DWORD (32-bit) of payload data

- Target Interface
 - o Very flexible, easy-to-use, high performance independent target write and read interfaces
 - o Supports 32-bit and 64-bit Memory Base Address Registers
- Register Interface
 - o Implements a 32-bit Memory Base Address Register for DMA and user registers
 - o Half of Base Address Register space is reserved for user registers
 - o Simple, fixed timing Register Interface makes adding user registers trivial

- Pre-integrated with other IP Cores to provide a full out-of-the-box PCI Express System Solution including:
 - o Reference design using PCI Express Core, PCI Express Back-End, Multi-Port Front-End SDRAM Core, and example Register and Target logic
 - o PCI Express Verification Suite
 - o Windows XP/Vista Driver and Example Application

o Linux Driver and Example Application

- Source code available
- Customization and Integration services available
- Expert technical support provided by core designers
- PCI Express™ Base Specification Revision 1.1 compliant

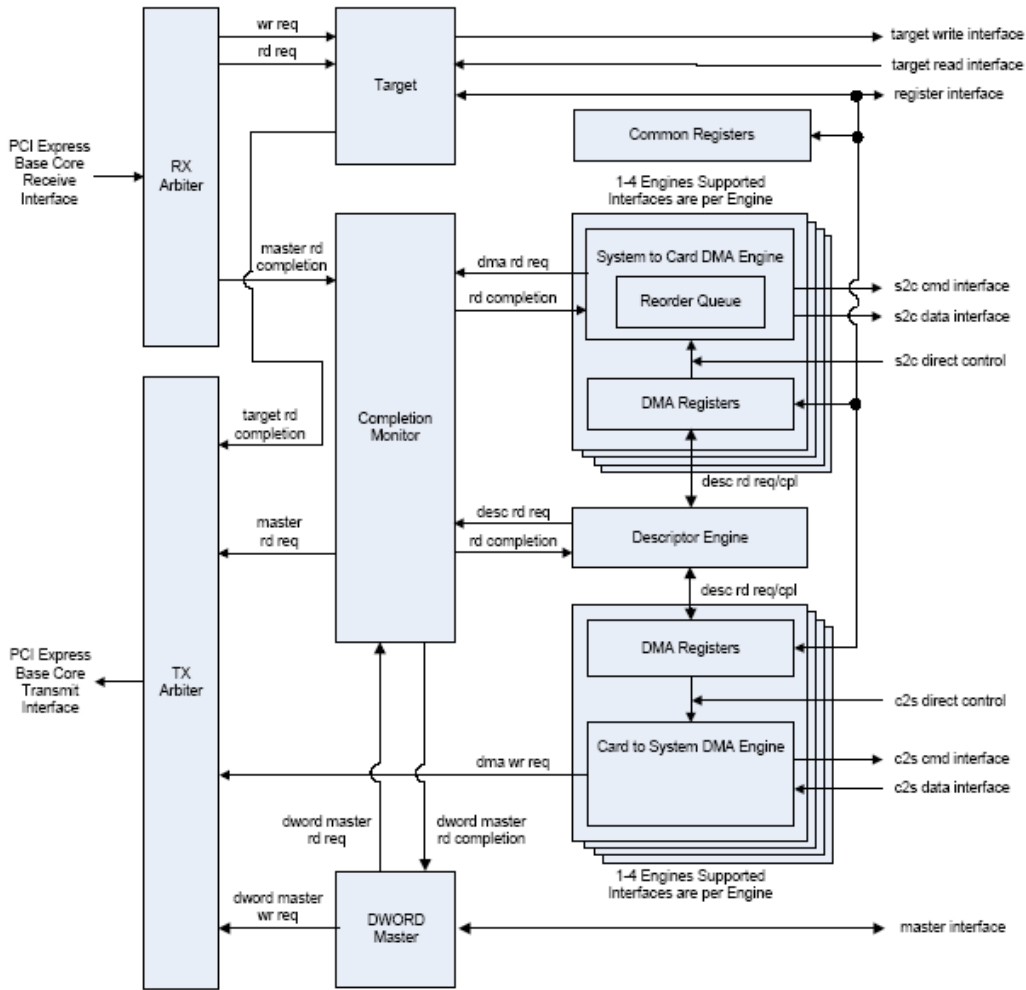


Figure (32) – PCI Express Back End Architecture

5.1.2) PCI Express Back-End Module Descriptions

• **RX Arbiter**

- o Arbitrates the base PCI Express core's receive interface
- o Received write requests are forwarded to the Target module for termination on the Target Write Interface or Register Interface
- o Received read requests are forwarded to the Target module for termination on the Target Read Interface or Register Interface
- o Received completions (read data resulting from master read requests) are forwarded to the Completion Monitor module for termination at the appropriate DMA/DWORD Master requestor

• TX Arbiter

- o Arbitrates the base PCI Express core's transmit interface
- o Transmitted write requests originate from Card to System DMA Engines/DWORD Master
- o Transmitted read requests originate from the Completion Monitor
- o Transmitted completions (read data/status from target reads) originate from the Target module

• Target

- o Generates the Target Write Interface for consuming received write requests
- o Generates the Target Read Interface for satisfying received read request
- o Generates the Register Interface for satisfying received write and read requests targeting the Base Address Register assigned to the PCI Express Back-End and user registers
- o Supports 32/64 Memory Base Address Registers

• Completion Monitor

- o Arbitrates among read requestors for PCI Express read request transmit resources
- o Manages limited PCI Express base core received completion buffer space
- o Re-associates received completions with the original request
- o Routes completion data to the original requestor

• DWORD Master

- o Completes read, write, and message requests initiated on the Master Interface
- o Processes read completions from read and I/O/Cfg write requests and returns data and status
- Common Registers
- o Implements centralized registers for DMA interrupts and global PCI Express Back-End capabilities

• DMA Registers

- o Implements the DMA registers for one DMA Engine
- o Registers are used by software to control and to obtain status from the DMA Engine
- o Processes DMA Chains; makes Descriptor read requests to the Descriptor Engine

• Descriptor Engine

- o Centralized resource for fetching Descriptors from system memory
- o Supports 32/64-bit address Descriptor Pointers

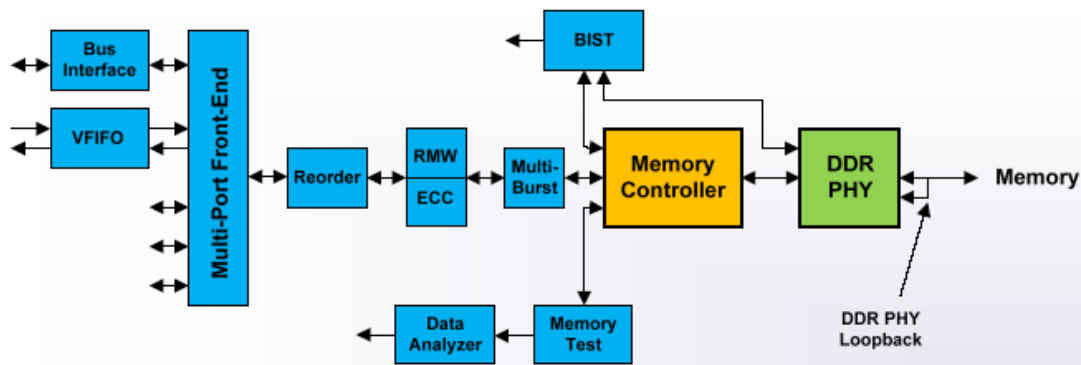
• Card to System DMA Engine

- o Takes DMA Data from user logic and transmits data to PCI Express using write requests
- o Executes the PCI Express and user logic transactions to fulfill a single Descriptor, returns status, and repeats as long as Descriptors are made available to execute
- o Accepts Descriptors from either the associated DMA Registers or from the DMA Direct Control Interface.
- o Supports 32/64-bit System and Card addresses of any byte alignment
- o Supports byte counts from 1 to $2^{32}-1$ bytes

• System to Card DMA Engine

- o Transmits PCI Express read requests and writes the resulting read completion data to user logic
- o Executes the PCI Express and user logic transactions to fulfill a single Descriptor, returns status, and repeats as long as Descriptors are made available to execute
- o Accepts Descriptors from either the associated DMA Registers or from the DMA Direct Control Interface.
- o Supports 32/64-bit System and Card address of any byte alignment
- o Supports byte counts from 1 to $2^{32}-1$ bytes
- o Implements a Reorder Queue to ensure that DMA read requests are returned in order (PCI Express Devices are permitted to reorder read transactions which is problematic for FIFO interfaces if not handled)

5.2) DDR 2 Memory Controller



The DDR2 SDRAM Memory Controller IP Core provides a high performance interface to DDR2 SDRAM devices. The DDR2 SDRAM Memory Controller IP Core accepts read and write commands using a simple Local Interface and translate these requests to the command sequences required by DDR2 SDRAM devices. The IP core also performs all initialization and refresh functions.

The DDR2 SDRAM Controller IP Core uses bank management techniques to monitor the status of each DDR2 SDRAM bank. Banks are only opened or closed when necessary, minimizing access delays. Up to eight banks can be managed at one time. Access cascading is also supported; allowing read or write requests to be chained together. This results in no delay between requests, enabling up to 100% memory throughput for sequential accesses.

The DDR2 SDRAM Controller IP Core is provided with run-time programmable inputs for all timing parameters (CAS Latency, tRAS, tRCD, tRRD, tRP, tRC, tRFC, tMRD, tXSNR, tFAW, tWR, tWTR) as well as memory configuration settings. This ensures compatibility with virtually any SDRAM configuration. The core is also available with hard coded timing and memory configuration parameters for designs requiring low logic utilization or for designs requiring high clock rate operation in slower FPGAs.

Core Deliverables:

- Core (Netlist or Source Code)
- Comprehensive Verification Suite (Source Code)
- Complete Documentation
- Expert Technical Support & Maintenance Updates

Available Add-on Cores:

- Bus Interface Cores
 - Support AHB, AXI (in development), Avalon, PLB (future)
- VFIFO Core
 - Turns a memory segment into a virtual FIFO
- Multi-Port Front-End Core
 - Provides a fully arbitrated, multi-port interface
- Read-Modify-Write Core
 - Handles writing non-aligned bursts into ECC protected memory
- ECC Core
 - Provides standard DRAM error detection / correction
- Multi-Burst Core

- Breaks extended bursts into multiple native memory bursts
 - Memory Test Core
- Performs a random address and data memory test
 - Data Analyzer Core
- Used to capture on-chip signals of interest such as the Memory Test data

Main Features:

- High performance access logic allows cascading of read and write requests enabling up to 100% throughput for all DDR2 burst length settings (4, or 8)
- Bank management logic monitors status of each SDRAM bank (up to 8 banks monitored) – banks only opened or closed when necessary, minimizing access delays
- Pipelined design enables high clock rates with minimal routing constraints
- Supports all standard SDRAM chips and DIMMs
- Run-time configurable timing parameters — CAS Latency (CL), tRAS, tRCD, tRRD, tRP, tRC, tRFC, tMRD, tXSNR, tFAW, tWR, tWTR. Timing parameters support operation up to 333MHz (667 Mb/s/pin)
- Run-time configurable memory settings (i.e. row bits, column bits, bank bits)
- Supports up to eight chip selects
- Support for DDR2 SDRAM device Self Refresh mode
- Support for DDR2 SDRAM device Power-Down mode
- Automatic generation of initialization and refresh sequences
- Commands may be issued with or without SDRAM auto-precharge – selectable at each transaction request
- Integrated data-path module for write DQS generation and read capture
- Core datapath tailored to FPGA family and/or ASIC library
- Optional Error Correction Coding ([ECC](#)), Read-Modify-Write (RMW) and Multi-Burst Modules available
- Source code license available (Verilog and VHDL) Architecture:

both for cases of short transfers to highly random address locations as well as cases of longer transfers to contiguous address space.

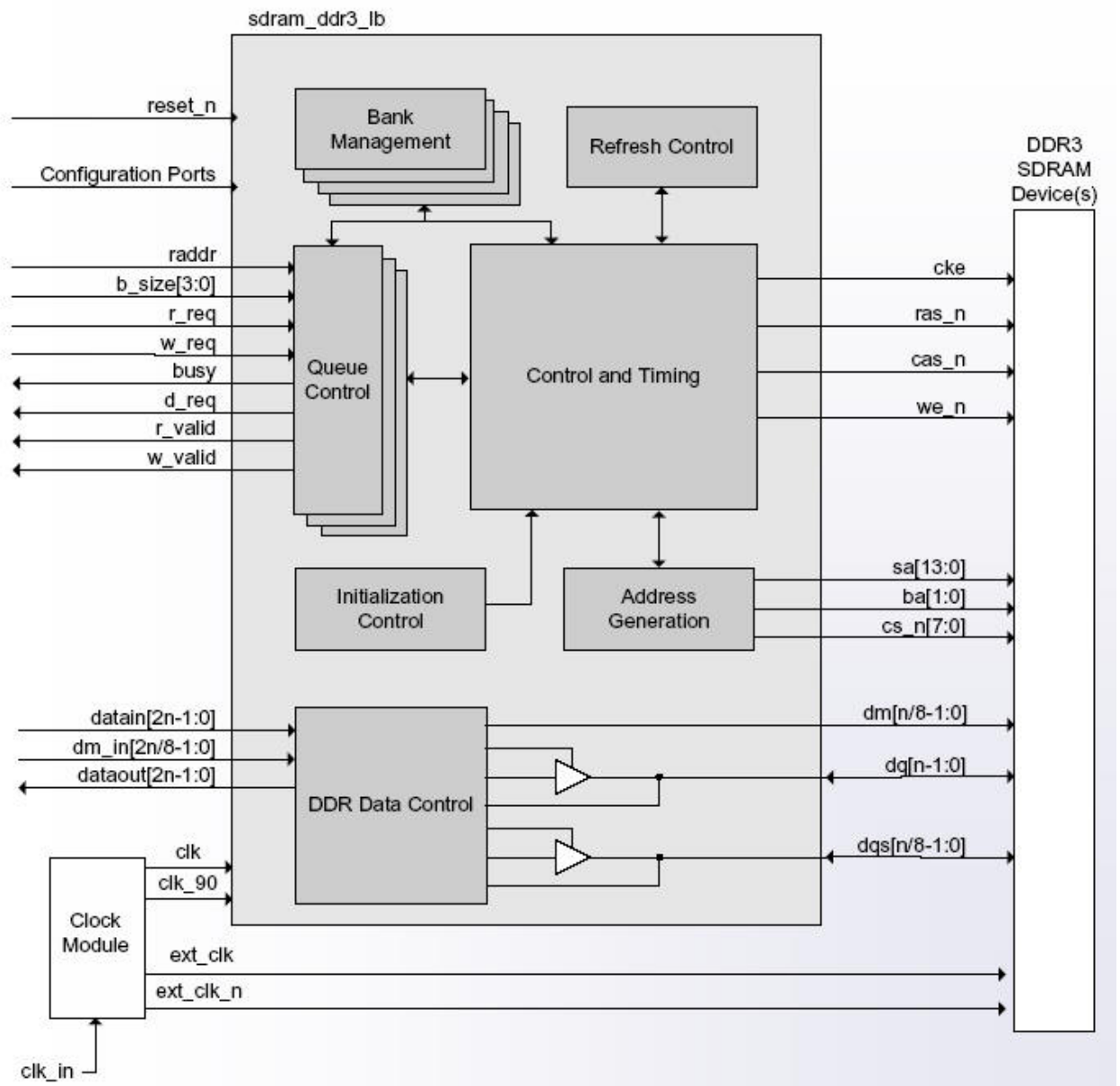
The core is provided with run-time programmable inputs for all timing parameters (tCL, tRC, tRCD, tRP, tMRD, tRRD, tRFC, tRAS) as well as memory configuration and refresh period settings. This ensures compatibility with all DDR2 SDRAM configurations.

Available Add-on Cores:

- Bus Interface Cores
 - Support AHB, AXI (in development), Avalon, PLB (future)
- VFIFO Core
 - Turns a memory segment into a virtual FIFO
- Multi-Port Front-End Core
 - Provides a fully arbitrated, multi-port interface
- Read-Modify-Write Core
 - Handles writing non-aligned bursts into ECC protected memory
- ECC Core
 - Provides standard DRAM error detection / correction
- Multi-Burst Core
 - Breaks extended bursts into multiple native memory bursts
- Memory Test Core
 - Performs a random address and data memory test
- Data Analyzer Core
 - Used to capture on-chip signals of interest such as the Memory Test data

DDR 3 SDRAM Memory Controller IP Core Features:

- Command queuing and bank management enable up to 100% memory throughput
- Supports auto-precharge commands for optimum random access performance
- Achieves high clock rates with minimal routing constraints
- Supports all standard DDR3 SDRAM chips and DIMMs
- Run-time configurable timing parameters and memory settings
- A variety of read capture options are supported
- Automatic generation of initialization and refresh sequences
- ECC, RMW and Multi-Burst add-on modules available
- Supports self-refresh and powerdown modes
- Source code available
- Customization and Integration services



P Core Deliverables:

- Core (Netlist or Source Code)
- Comprehensive Verification Suite (Source Code)
- Complete Documentation
- Expert Technical Support & Maintenance Updates

Technical Support:

Technical support can be provided by contacting support@HiTechGlobal.com. Support requests are responded in less than 24 hours.

Sales Support:

Sales support can be provided by contacting info@HiTechGlobal.com or +1 408 781-8043 (8:00 AM – 6:00 PM Pacific Standard Time)