A. Reference Design Details

A.1 Overview

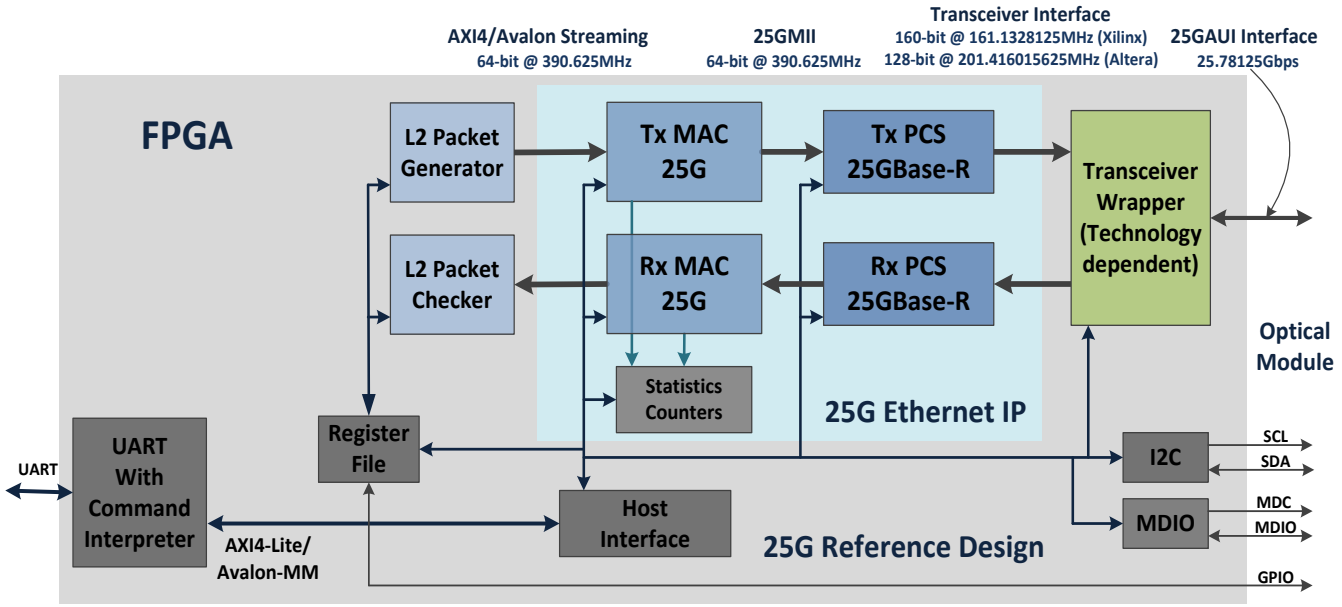
A 25Gbps reference design is included as part of the IP deliverable to facilitate quick L1 and L2 layer testing and verification of the 25Gbps Ethernet on target platform. The capability to run the L1 PRBS pattern and configure each transceiver independently can be for used for a fast module bring-up in the lab and can also be used for factory diagnostics.

The UART (normally through an onboard USB-to-UART converter chip) based 25G Ethernet reference design can be seamlessly ported to various COTS FPGA networking and evaluation modules (see section for the list of verified modules). A GUI application controls the register read/writes to the FPGA through a UART core with integrated command interpreter. Both Linux and Windows platforms are supported for the UART based interface control.

This reference design can also be used on custom embedded design where the FPGA connects to the host processor via a PCIe interface. For the PCIe control interface, GUI application is hosted on a Linux platform (as PCIe driver/API is provided for Linux OS only).

A.2 Functional Description

Following figure shows the connectivity and the elements of the 25Gbps Ethernet IP reference design. Usually the UART interface from the FPGA connects to an external (can be on the same module as well) USB-UART converter. A Linux host (embedded or standard PC) running a GUI application is used to configure and control the 25G Ethernet. I2C and GPIO interfaces included in the reference design can be used to control any optical module on the target platform including the XFP+ and XFP compliant modules.



For L1 (physical layer verification and testing) GUI application provides an interface to independently control and configure 25.78125Gbps transceiver used for 25G Ethernet transport. User can configure the transceiver to run various PRBS pattern and configure various transceiver parameters like transmit voltage, transmit pre-emphasis, receive equalization and receive gain.

For L2 testing, GUI application uses the 25Gbps packet generator/checker inside the FPGA to generate and check MAC frames up to full line rate. Packet generator supports a basic rate control mechanism to control the packet/data rate on the interface. Generator can be configured for fixed size as well as pseudo random packet size packet transmission. An incrementing counter is used as payload for the MAC frames. Checker on the receive side verifies the payload of receive MAC frames and reports error in the payload.

A comprehensive set of transmit and receive counters in the MAC core provide a detailed view of the packet statistics including various error types.

Following is a snapshot for the GUI application for the L2 packet test results screen.