

Product Description:

The ML361 Virtex-II Pro DDR400/PC3200 Memory Board provides a communications platform between a Virtex-II Pro FPGA and high-speed double-data-rate (DDR) memories with operating speeds up to 200 MHz. The ML361 has three major functions:

- Tests and verifies the interoperability of Virtex-II Pro devices with high-speed DDR memories.
- Serves as a development platform for Xilinx and its customers to use for building memory controllers
- Provides a means by which Xilinx can demonstrate high-speed DDR memory interoperability.

The ML361 demonstrates a 64-/72-bit interface to a 128 MByte, 200 MHz DDR SDRAM DIMM, a 72-bit interface to five 256 Mbit, 200 MHz DDR SDRAM components, and an additional 8-bit, 166 MHz interface to a 256 Mbit DDR SDRAM component on one of the top banks.



Main Features:

- One Virtex-II Pro FPGA (XC2VP20FF1152-6)
- One DDR SDRAM DIMM (MT4VDDT1664-AG-40BC3) - 128 MBytes / 64-/72-bit data interface
- Five DDR SDRAMs (four MT46V16M16TG-5B devices and one MT46V32M8TG-5B device) - 1.28 Gbits / 72-bit data interface
- One DDR SDRAM (MT46V32M8TG-5B) - 256 Mbits / 8-bit data interface
- Two separate controllers for each 72-bit memory interface
- 200 MHz interface
- The memory interfaces are located on the FPGA left/right interface and top I/O banks (banks 1, 2, 3, 6, and 7)
- 1x Serial Port
- 2x MICTOR (38-pin)
- 2x GPIO Headers
- 2x SMA Connector (External Clock)
- Power Supply (5 V)
- JTAG - PIII
- JTAG - PIV
- Clock 200 MHz and 166 MHz
- Push, Program, and Reset Buttons
- DIP Switch
- 7-Segment Display
- PROM

Ordering Information:

Part Number: HW-V2P-ML361

Price: \$3,500

Kit Content:

- Xilinx Virtex-II Pro ML361 Platform
- Power Supply
- Memory Controller IP Core

